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A Fully Programmable DAQ Board of Vibrational Signals from IEPE Sensors: Hardware and Software Design, Performance Analysis

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Abstract: Vibration analysis is commonly used to assess machinery conditions, earthquake detection, and structural monitoring. Commercially available DAQs (Data Acquisition Systems) feature high costs and limited versatility in terms of end-user hardware/firmware customization, making it difficult to adapt them to the input signal features and add supplementary functionalities. Hence, this research aims to develop a custom acquisition board for detecting vibration signals via IEPE (Integrated Electronic Piezoelectric) sensors, considering the limitations of commercially available systems, and building upon solutions found in the literature. The DAQ board was intended for remote vibration monitoring of infrastructure and machinery for industrial applications, allowing the implementation of predictive maintenance strategies. The proposed DAQ board has two independent and fully configurable channels, which can be set for acquiring signals from IEPE sensors or generic voltage sources. The DAQ board relies on the STM32F401 microcontroller to manage the acquisition from high-speed ADCs, process data, and store them in mass memory (SD card). During acquisition, the DAQ implements a batch acquisition strategy based on a buffer flash memory for temporarily storing ADCs data, which are iteratively poured into mass memory. Also, the board has Bluetooth connectivity to transmit acquired data and receive commands remotely. A prototype of the DAQ board was developed and tested with several waveforms, including vibration signals. The tests showed that the board can acquire vibration signals and compute the FFT onboard. The DAQ demonstrated a good balance between performance, accuracy, flexibility, and cost, making it suitable for several industrial applications and allowing for scalability and integration potential.

Keywords: vibration analysis; structural monitoring; IEPE sensors; DAQ board; signal conditioning; onboard FFT

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Citation: De Fazio, R.; Spongano, L.; Messina, A.; Visconti, P. A Fully Programmable DAQ Board of Vibrational Signals from IEPE Sensors: Hardware and Software Design, Performance Analysis. *Electronics* **2024**, *13*, 1187. https://doi.org/10.3390/electronics13071187

Academic Editors: Ajit Jha, Ioan Burda and Carlos Cruz

Received: 14 February 2024
Revised: 20 March 2024
Accepted: 21 March 2024
Published: 24 March 2024

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1. Introduction

Vibration analysis is a versatile tool for assessing the mechanical integrity of various types of machinery and for scientific applications, such as earthquake magnitude estimation [1]. This technique also evaluates specific parameters, including vehicular comfort and engine performance. Forced vibration tests are particularly useful for structural monitoring, which involves the real-time assessment of key parameters related to structures, buildings, or industrial machinery to identify potential risks or damage [1–3].

Various vibrational characteristics (e.g., relative displacement, velocity, story drift, vibration frequency, damping, or tilt) can be effectively monitored using accelerometers, offering a comprehensive view of the structural dynamics under investigation [4].

In the context of rotating machinery, vibrations are an inherent byproduct of operation [5]. Measuring these vibrations is central to condition monitoring (CM), which is a proactive maintenance strategy that enables maintenance decisions to be predicated on

the actual mechanical state of the machinery rather than its operational runtime. This approach significantly reduces time, effort, and associated costs. Each component within a machine vibrates at its natural frequency. These vibrations are transmitted through corresponding parts of the machinery. This phenomenon results in a unique vibration signature that indicates the machine's healthy operational state. When a fault arises, the frequency components within the vibration spectrum change, producing a distinct vibration pattern. Consequently, vibration data can be analytically correlated to physical processes, providing insight into the overall health of the equipment.

However, the main drawback of this approach is the stringent specification requirements for the acquisition equipment, encompassing factors such as precision, resolution, sampling frequency, and channel number [6]. Additionally, the associated costs can be prohibitive; commercial data acquisition systems for vibration analysis can cost upwards of EUR 3500–4000 for high-end single-channel instrumentation. These systems often employ multiple channels connected to a single Analog-to-Digital Converter (ADC), resulting in crosstalk and limited sampling frequencies. Moreover, they also offer restricted hardware and firmware customization options, lacking features like Variable Gain Amplifiers or advanced digital processing techniques. Therefore, these motivations have pushed the scientific community to look for alternative and customized DAQ solutions, characterized by lower costs, improved performances, and a wider range of functionalities tailored to each specific application (machinery monitoring, structure monitoring, automotive suspension monitoring, etc.) [6–8]. Different works were proposed in the scientific literature to overcome these limitations, including low-cost microcontroller sections and commercial inertial sensors, supporting the previous motivations and extending the functionalities and processing capabilities compared to DAQ solutions available on the market.

Various sensor technologies are available for vibration monitoring, including piezoelectric (PZT) sensors, micro-electromechanical sensors (MEMS), proximity probes, and laser Doppler vibrometers [8–10]. PZT sensors are particularly prevalent, as they generate voltages when subjected to deformation. These voltages can be digitized and translated into vibration signals. Specifically, Integrated Electronic Piezoelectric (IEPE) sensors are the most commonly used vibration sensors in industrial settings.

This research presents a custom Data Acquisition System (DAQ) for detecting vibration signals via IEPE sensors, considering the limitations of commercially available systems and building upon solutions proposed in the existing literature. In detail, the proposed DAQ is designed to act as low-cost sensor nodes for vibration monitoring of infrastructure and machinery by IEPE sensors to early detect failures and malfunctions. From the perspective of Industry 4.0, several sensor nodes can be distributed in an industrial scenario to monitor different machinery discreetly and accurately, ensuring versatility and reconfigurability. The proposed DAQ board could be used in predictive maintenance scenarios; in fact, the vibration signal analysis allows for reduced downtime and cost savings in industrial settings. Indeed, the presented DAQ board is equipped with wireless connectivity (Bluetooth) for transmitting acquired data and receiving commands from a remote host device, enabling installation in narrow or difficult-to-access places. Hence, the custom DAQ to be developed aims to meet the following specifications, not met simultaneously by existing commercial or academic solutions, at a relatively reduced cost: 14-bit resolution; two independent acquisition channels, each equipped with a single ADC; input filtering availability; support for external memory; and onboard Fast Fourier Transform (FFT) computation. This last functionality is an advantage making available at the source, the essential information to perform a modal analysis without post-processing by an external computing device (e.g., a PC).

The designed DAQ board has the following features:

- 14-bit resolution.
- Two independent acquisition channels, each with a single ADC and user-selectable input ranges.
- VGAs with gains ranging from 1 to 600 V/V.

- Antialiasing Sallen–Key low-pass filters for each channel
- Maximum sampling frequencies of 12.5 kHz for dual-channel operation and 22.2 kHz for single-channel operation.
- Onboard Fast Fourier Transform (FFT) capabilities.
- Micro-SD card support for data storage.
- Two user-configurable acquisition modes for each channel: "MODE 1" for generic vibrational signals and "MODE 2" for IEPE signals.

The proposed DAQ system relies on commercial boards and ICs for conditioning, acquiring, and processing the signals from IEPE sensors or generic signal sources, resulting in a general-purpose tool for supporting studies in structural and machinery monitoring featuring high flexibility from hardware and firmware points of view, simplicity in assembly, and reduced costs; indeed, the developed DAQ board is fully configurable, enabling it to be adapted to different typologies of IEPE sensors and voltage sources.

The DAQ's core is an STM32F401CC microcontroller for acquiring and processing the data from IEPE sensors, ensuring high performance and flexibility. Furthermore, the proposed DAQ board comprises a reconfigurable conditioning section for supplying and managing the signals from IEPE sensors and other signal sources, making them suitable for the following acquisition by a 14-bit ADC for each acquisition channel. A proper firmware was developed for the developed DAQ, which performs a batch acquisition strategy, temporarily storing data in a buffer flash memory and periodically pouring data into the mass memory represented by the micro-SD card for post-processing. A DAQ board prototype was deployed to test the developed firmware strategy, validating this approach for the proposed application and demonstrating that it ensures low data loss; also, by acting on firmware, the sampling frequency can be changed to adapt them to the spectral content of the input signal. For this purpose, a description of the developed firmware is reported, detailing the main methods for managing the acquisition, processing, and storage of the acquired data. Unlike similar work reported in the scientific literature, the proposed DAQ board uses IEPE sensors, not MEMS sensors, characterized by a wider operating range and higher robustness required for industrial applications [1,11].

The board achieves a good balance between performance, accuracy, and flexibility, allowing for versatility in different industrial applications. A comparative analysis of the proposed general-purpose DAQ with similar ones reported in the scientific literature was carried out from the point of view of resolution, sampling frequency, number of channels, availability of variable gain amplifiers, use of a dedicated ADC for each channel, onboard FFT computation, and accuracy. It suggested that the proposed DAQ system ensures higher flexibility and broader functionalities than similar works reported in the scientific literature. The system design allows for easy scalability and integration, which could be advantageous in large-scale applications requiring multiple sensor nodes. The above-mentioned features and onboard FFT computation capabilities make the designed board comparable to commercial solutions. Moreover, the board's design allows for future firmware updates. The costs of the designed board are approximately EUR 400–500, significantly lower than the commercial systems, which, as stated before, can cost upwards of EUR 3500–4000. The main contributions and novelties of the proposed paper are:

- Hardware and firmware development of a custom and fully reconfigurable DAQ for acquiring signals from IEPE sensors of generic signal sources for structure and machinery monitoring. The developed solution relies on commercial boards and ICs to ensure simplicity in assembly, reduced costs, and high flexibility.
- Firmware implementation of the batch acquisition strategy is based on a buffer flash memory for temporarily storing acquired samples from the ADC, which are iteratively poured into a mass memory, represented by a micro-SD card.
- Realization of the DAQ prototype to test the developed firmware strategy, demonstrating its effectiveness in acquiring generic signals.

The remainder of the paper is organized as follows: Section 2 describes the hardware architecture of the developed board. Section 3 addresses the realization of the DAQ proto-

type to validate the proposed architecture. In Section 4, the tests on the developed DAQ prototype are described. Lastly, Section 5 summarizes the main technical specifications of the proposed DAQ board (in table form) and discusses the main results of the board design and experimental tests.

1.1. Related Works

Several data acquisition systems for monitoring and analyzing vibrational signals provided by inertial sensors have been introduced in the literature. In this paragraph, an overview of these systems will be presented. Among the DAQ systems proposed, several employ generic piezoelectric accelerometers as their sensing stage to acquire vibrational signals. C. R. Soto-Ocampo et al. developed a multi-channel data acquisition system sufficiently compact to be located in places of difficult access [3]. This system comprises a microcontroller unit, an external ADC, and a low-cost piezoelectric accelerometer (Figure 1).

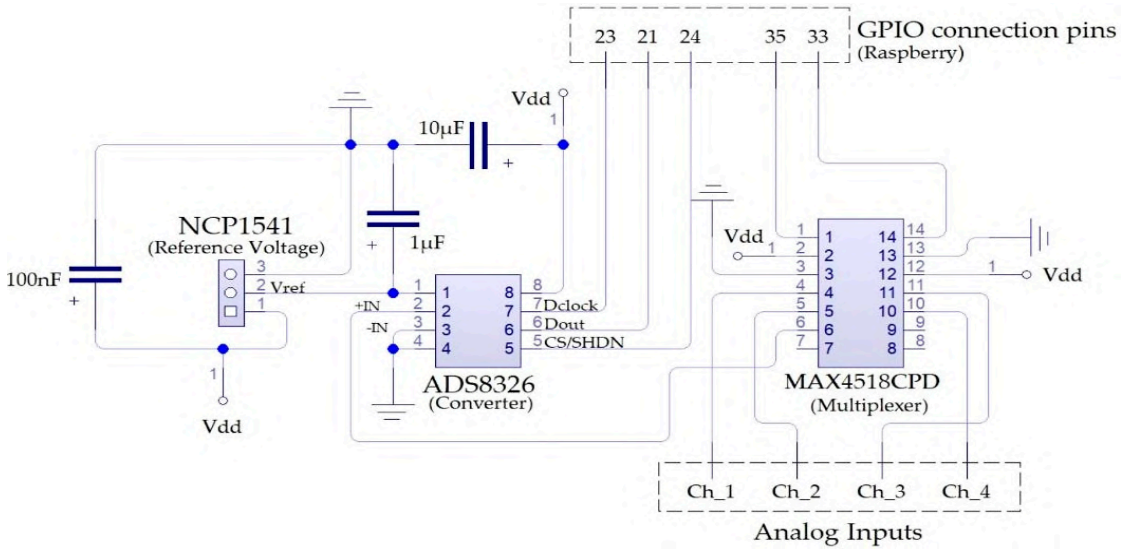


Figure 1. Schematic of the DAQ board presented in ref. [3].

The SPI protocol between the microcontroller and the ADC is used to achieve high operational speed. A sample and hold (SH) circuit is implemented through an analog multiplexer to select the channel with a higher amplitude. Moreover, the implemented firmware relies on a multi-thread system for setting ADC, acquiring data, and estimating the time interval in which the data are written. The sampling frequencies of this DAQ are 110, 65, 45, and 35 kHz using 1, 2, 3, and 4 channels, respectively. S. M. Shyni et al. designed a virtual instrumentation-based DAQ for vibration monitoring and analysis, which consists of three main sections: a piezoelectric sensor, signal conditioning, and microcontroller-based processing, including a low-power 8-bit ADC and an embedded microcontroller [12]. R. S. Mathad et al. designed a low-cost multi-channel DAQ based on operational transconductance amplifiers (OTAs) and OTA-based filters to acquire and process signals from a piezoelectric accelerometer [13]. Several DAQ section prototypes are presented in the literature for gathering signals from IEPE sensors. A. Villarroel et al. developed a low-cost single-channel vibration measurement system for IEPE sensors with a 20 kHz sampling frequency consisting of analog and digital sections [14]. The former includes sensing and conditioning blocks (Figure 2a); the latter comprises microcontroller-based acquisition, processing, storing, and networking sections (Figure 2b).

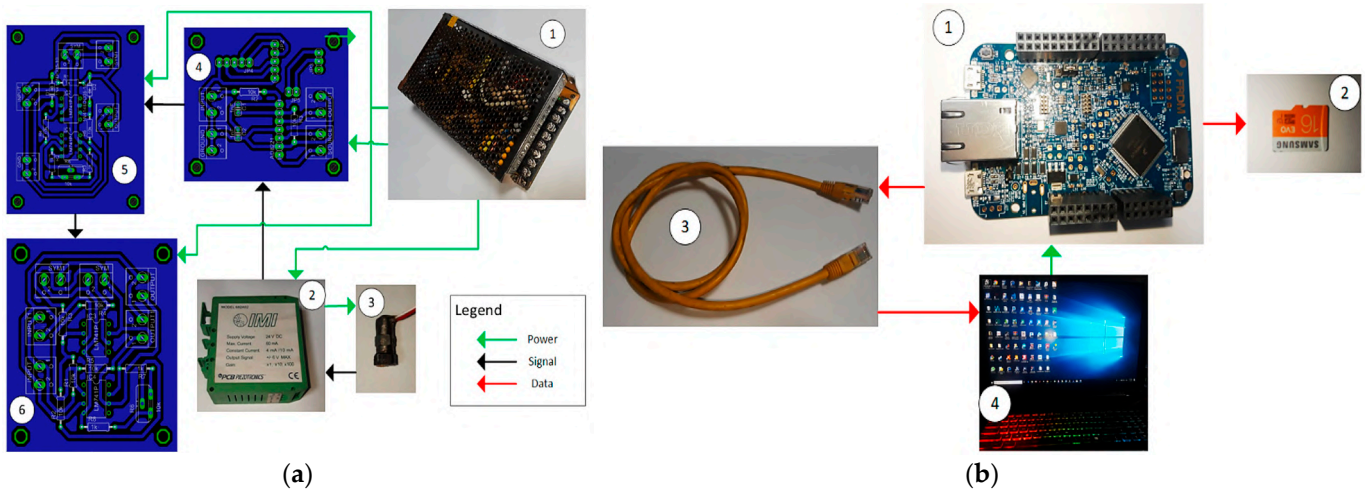


Figure 2. Analog section (**a**) of the system proposed in ref. [14] with highlighted the power supply (1), signal conditioner (2), accelerometer (3), active antialiasing filter (4), diode clipper circuit (5), and the Direct-Current voltage bias circuit (6); the digital section (**b**) of the designed solution with highlighted the development board (1), MicroSD card (2), Ethernet cable (3), and the laptop (4).

H. Guo et al. developed a vibrational analysis system, including 8 independent IEPE sensors and signal conditioning sections [15]. It includes 16-bit ADC with 8 channels, supporting a maximum throughput of 200 kSPS on each channel. The developed firmware manages the acquisition and processing of vibrational data and their transmission to a PC through Ethernet for post-processing. S. Hu et al. proposed a vibration monitoring system employing a Cortex-M3 MCU, a sensor modulation circuit, and an IEPE accelerometer [16]. The 12-bit ADC embedded in the microcontroller digitizes the IEPE sensor's signal. Furthermore, a filtering stage, which consists of a high-pass and a low-pass filter, is implemented to reduce noise interference. Finally, the sensor modulation circuit's output is connected to the microcontroller's ADC, delivering the acquired data to a PC via a UART (Universal Asynchronous Receiver Transmission) interface. In addition, A. Toscani et al. developed a scalable and reconfigurable data acquisition system for monitoring industrial machinery [17]; this last one comprises a central node connected to several subnodes communicating through an A^2B bus, each collecting up to four channels from embedded IEPE. The presented system reaches up to 48 kSPS over 32 channels, ensuring good synchronization of all signals independently from their source.

Also, the wireless communication capability of DAQ boards for vibration monitoring is another precious feature for structure and machinery monitoring applications, considering that the application areas are usually narrow and difficult to reach. For instance, in [9], O. Zobel et al. designed and realized an open-source data acquisition board for IEPE sensors called OASIS, based on widely accessible parts and a broadly community-supported microcontroller (ESP32 family). It features four channels for IEPE signals with 20 kHz and 16-bit resolution. Furthermore, wireless synchronization of multiple data acquisition devices is implemented. An experimental validation indicates that coordinating both systems employing this approach with a latency lower than 100 µs is feasible.

Other systems utilize MEMS accelerometers as a sensing stage for acquiring vibrational signals. Gopalakrishna et al. implemented a low-cost system for monitoring rolling bearings using a 3-axis piezo-capacitive MEMS accelerometer [11]. A microcontroller section acquires data from the MEMS sensor with a 1 KSPS sample rate and transfers them to a PC through the UART interface. A MATLAB-based script implements wavelet-based denoising algorithms and time-domain and frequency-domain analyses of the acquired data to extract kurtosis and energy. I. A. Jamil et al. developed a single-channel, low-cost vibration monitoring system with a 10-bit resolution ADC with a configurable sampling rate [1]. The hardware section includes a microcontroller, a 3-axis MEMS accelerometer,

and an integrated circuit for the RS232 interface. The system's performance concerning the frequency domain is limited by the implemented sensor's frequency response, i.e., from 0.5 Hz to 1.6 kHz on both the x and y axes and from 0.5 Hz to 550 Hz on the *z*-axis.

K. Gürkan et al. implemented a low-cost and battery-powered wireless data acquisition system with multiple acquisition channels based on tri-axial MEMS accelerometers that use Bluetooth (namely, IEEE 802.15.1) protocol for data transmission [2]. An 8-bit low-power microcontroller acquires the accelerometer data with a 100 Hz sample rate and communicates with the Bluetooth module. Y. Gorbounov and T. Dzhikov developed a low-cost DAQ for the condition monitoring of electric motors that employs a MEMS accelerometer that constitutes the system's sensing section and an FPGA-based (Field Programmable Gate Array) microcontroller [18]. The microcontroller embeds a 12-bit ADC with a cumulative output rate of 1 MSPS. The data analysis is carried out through an external program developed in Python and intended for machinery vibration analysis in both the time and frequency domains.

1.2. Analysis of Commercially Available DAQs for Vibration Analysis

This section reviews commercially available solutions for vibration acquisition and analysis, i.e., the NI 9233/9234 acquisition boards, the DELPHIN Expert Vibro data acquisition boards, the ADASH A4900 Vibrio M vibration monitoring device, and the WebDAQ 504 system. The NI 9233 and NI 9234 (produced by National Instruments Inc., Austin, TX, USA) are four-channel DAQs used for high-accuracy vibration measurements from IEPE sensors [19]. The boards of this series present an IEPE signal conditioning stage consisting of a 2 mA constant current reference. The NI 9234 has three different software-configurable modalities of operation for the measurements: IEPE-on with AC coupling, IEPE-off with AC coupling, and IEPE-off with DC coupling [19]. However, the NI 9233 features only IEPE excitation and AC coupling, which is always enabled and not software-configurable. The four input channels acquire data simultaneously with an adjustable sampling frequency between 2 and 50 kHz. These DAQs use the delta-sigma modulation method of analog-to-digital conversion, which allows the actual sampling frequency of each ADC to be 128 times the sampling frequency set by the user. The board includes the following components: a voltage buffer, an analog pre-filtering stage, a 24-bit ADC, and an additional antialiasing digital filter with a user-configurable cut-off frequency, which expands the data to 24 bits and then rejects the signal frequency components greater than the cut-off frequency. Subsequently, the data are digitally resampled at the selected data rate.

The DAQs of the Expert Vibro family (manufactured by Delphin Technology AG, Bergisch Gladbach, Germany) are devices used to acquire vibration signals [20]. For instance, the Expert Vibro EV 16 features 16 synchronous channels, whereas the EV 8 and EV 4 models feature 8 and 4 channels, respectively. These systems present a dual-core FPGA processor based on ARM technology. Each acquisition channel of the Expert Vibro systems incorporates an independent 24-bit ADC. In addition, the sampling frequency is adjusted by software between 1 Hz and 50 kHz independently for each channel [20]. Furthermore, these systems include integrated comparators and digital inputs that allow individual triggering of each ca 32 GB of memory for data storage. These systems also allow users to compute up to 12,800 spectra lines through the FFT and include signal processing functions. Expert Vibro systems have several interfaces, enabling the board to be connected to the intranet/internet and computers via USB ports.

The A4900 VIBRIO M vibration monitoring device (manufactured by Adash s.r.o., Ostrava, Czech Republic) allows for the execution of all basic vibrational diagnostic measurements [21]. This system includes a single channel whose input consists of a single IEPE accelerometer, characterized by a 100 mV/g sensitivity and a 60 g peak input range. This DAQ can acquire velocity signals within the 1 Hz and 1 kHz frequency ranges and acceleration signals between 1 Hz and 16 kHz. The system has a memory size of 4 MB, which is used for data storage. This way, the storage of 900 measurements of 800 lines of

the spectrum or, if time-domain measurements are chosen, 2048 sample time signals are possible. The system is capable of off-route and route measurements.

The WebDAQ 504 (manufactured by Measurement Computing Inc., Norton, VA, USA) is a DAQ designed for acoustic and vibration signals and allows remote monitoring and control [22]. The system is equipped with a single sigma-delta ADC with a 24-bit resolution. Thus, the system can acquire data simultaneously from up to four analog inputs, whose sampling frequency can be up to 51.2 kHz for every channel. Furthermore, each input can be configured for either voltage or IEPE sensor measurements; in the former case, the user can select the coupling between AC or DC. The DAQ provides a minimum excitation current equal to 4 mA and an IEPE compliance voltage up to a maximum of 19 V for driving the internal circuitry. Moreover, the system is capable of computing FFTs in real time; in this way, continuous monitoring and analysis of the signals are possible. The user can initiate or finalize the acquisition considering FFT, analog, or digital thresholds, alarm states, or time/date values. The system supports on-demand push-button triggering. In addition, the user can store data files or configuration settings in internal flash memory or save them to external network or media folders.

2. Architecture of the Proposed Acquisition Board

The proposed DAQ board has two channels, each featuring two user-selectable operating modes. The first one ("MODE 1") is intended for general-purpose vibration signals provided by a function generator or acquired by an accelerometer (Figure 3). The signal conditioning chain consists of a voltage buffer and a VGA to amplify the buffer output to match the ADC input range, equal to $\pm$10 V in "MODE 1". The voltage buffer is realized using the OPA27GP op-amp (manufactured by Texas Instruments Inc., Dallas, TX, USA) [23] and the VGA is realized using the LT1037ACN8 op-amp (manufactured by Linear Technology Inc., Milpitas, CA, USA) [24]. The second operation mode ("MODE 2") is designed for vibration signals provided by IEPE accelerometers (model 333B32, manufactured by PCB Piezotronics Inc., Depew, NY, USA) (Figure 3). This acquisition chain includes a current generator because IEPE accelerometers require a constant current and a controllable level shifter based on the OPA27GP op-amp. This transforms the sensor output to a signal in the range 0 V $\div$ + 10 V. The shift voltage is controlled through a potentiometer (Figure 3).

The PCB model 333B32 is a shear typology IEPE sensor whose sensing element is a ceramic material [25]. It has the following dimensions: 16 mm in length and 10.2 mm in width, and it supports 10–32 coaxial jacks as electrical connectors. The main features of the sensor are the following: 100 mV/g sensitivity, measurement range equal to $\pm$50 g, 0.5 Hz to 3 kHz frequency range, excitation voltage from 18 V to 30 V, output bias voltage from 7 V to 12 V, and a constant current excitation in the range from 2 mA to 20 mA (Figure 3).

A voltage limiter is included before each acquisition chain mentioned above to protect the board from sudden damaging voltage spikes.

Once the user has selected the operation mode, the output of one of the acquisition chains is connected to a low-pass Sallen–Key antialiasing filter based on the OPA27GP. Then, the filtered signal is digitized through a dedicated ADC for each channel. After the trigger signal is provided to the MCU, it simultaneously sends a "start of conversion" (SoC) signal to the two ADCs. Once the conversion process carried out by one ADC ends, the MCU receives its corresponding "end of conversion" (EoC) signal. Once the conversion process has ended for both ADCs, the MCU will sequentially acquire the digital words from the output of the two ADCs. In detail, the MCU is interfaced through an SPI bus with the two ADCs. The acquisition board stores the acquired data on an SD memory card; in particular, the SD module is connected to an independent SPI bus to avoid firmware conflicts during the data storage. Furthermore, the MCU can exchange data with an external PC through a UART interface and wirelessly transmit them through a Bluetooth module connected to another independent UART interface (Figure 3).

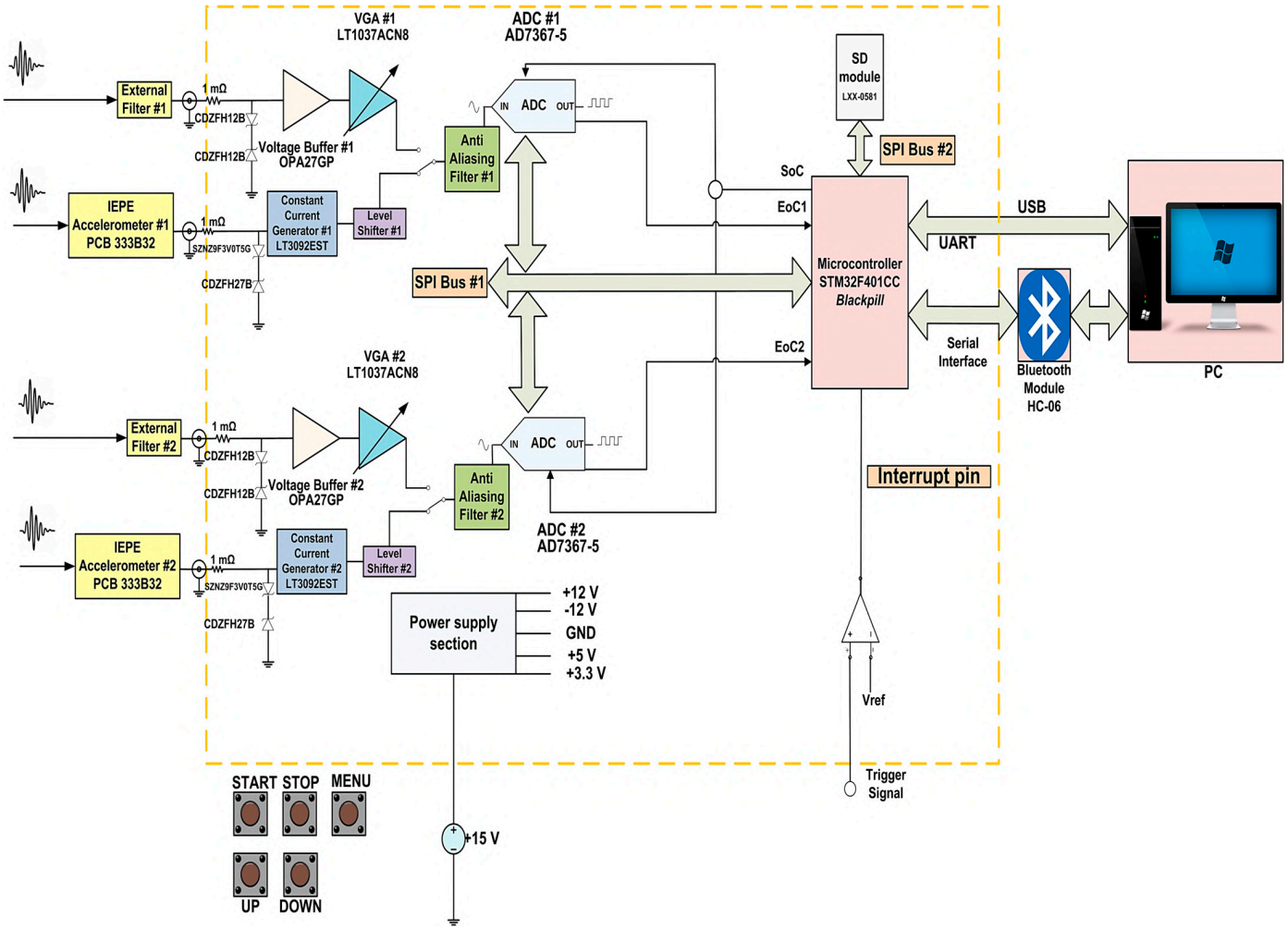


Figure 3. Block diagram for the proposed acquisition board.

Moreover, the board comprises a power supply section that provides the supply voltages to all circuitry included on the board; specifically, +15 V and +26 V are provided to the board through external suppliers, and then the power supply section will generate the following voltages through cascaded voltage regulators: +12 V, −12 V, +5 V, and +3.3 V. A comparator is used to generate a digital waveform from the external trigger signal employing the reference voltage V_{REF}; the resulting signal is connected to an interrupt pin of the MCU. Furthermore, the acquisition board includes five buttons connected to as many MCU GPIOs as possible for providing commands to the microcontroller.

2.1. Design of the Signal Conditioning Chain for "MODE 1"

The "MODE 1" signal conditioning chain consists of a voltage buffer, which shifts the input signal to a low-impedance node, and a VGA that makes the buffer output fit the ADC input range. The input range must be set to ±10 V in this operation mode.

The acquisition chain is preceded by a voltage limiter consisting of two anti-series Zener diodes (i.e., CDZFH12B), whose absolute value of the Zener voltage $|V_z|$ equals 12 V, and a 1 mΩ series resistor. In this way, the input signal is limited in the range $\pm(|V_z| + V_\gamma)$V, where V_γ is the forward bias voltage (Figure 4). The voltage buffer is based on the OPA27GP op-amp, which features low noise, low offset, and adequately high bandwidth for the

desired application. The proposed VGA is based on the LT1037ACN8 op-amp and relies on the non-inverting configuration, whose closed-loop gain A_V is equal to:

$$A_V = \left(1 + \frac{R_f}{R_1}\right), \quad (1)$$

Rf is the feedback resistance, and R1 is the resistance at the non-inverting terminal of the op-amp. Therefore, different gains can be obtained by varying either R_f or R_1 (Figure 5).

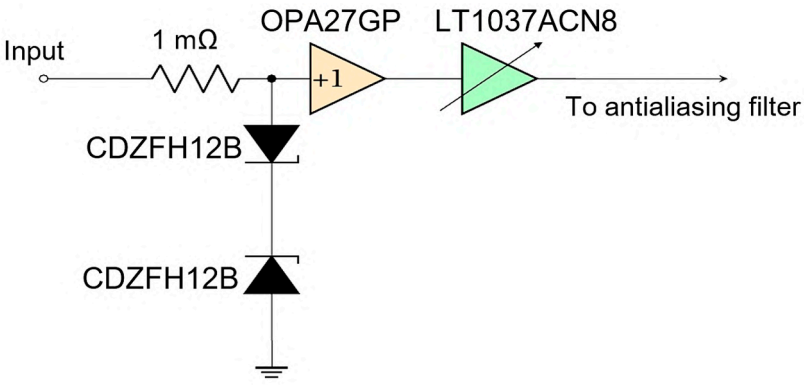


Figure 4. Functional block diagram for the signal conditioning chain for "MODE 1".

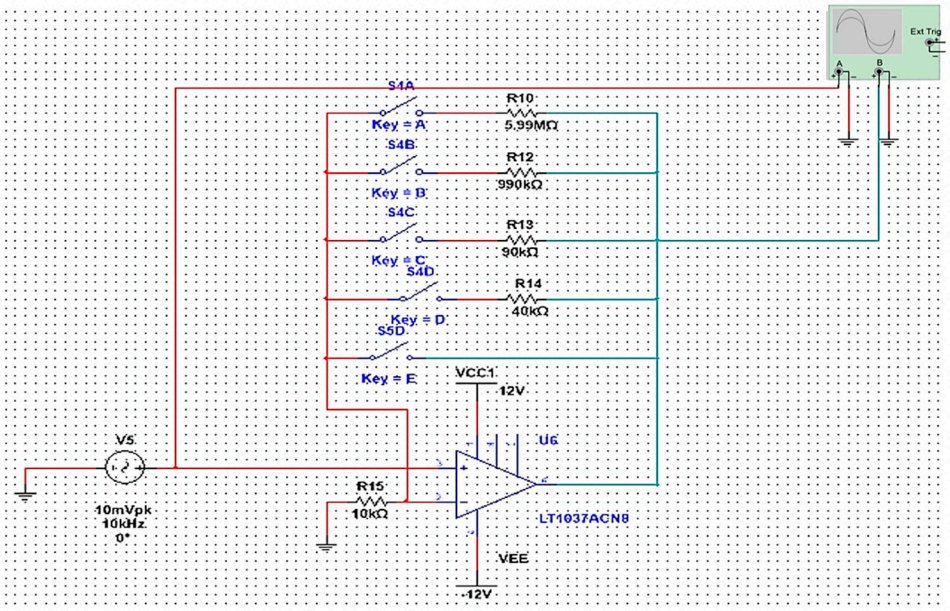


Figure 5. Multisim setup for the implemented VGA. The VGA is designed assuming a sinusoidal input signal with a 10 mVpk amplitude and a 10 kHz frequency as the input.

In this application, the different gains are obtained through the variation of R_f, whereas R_1 is set to 10 kΩ. Specifically, R_f is constituted by four different shunt resistances (R_{f1}, R_{f2}, R_{f3}, and R_{f4}) and a short circuit connection (if this connection is enabled, the VGA behaves like a voltage buffer), whose combination can be set by the user through the insertion of jumpers in the corresponding positions. The feedback resistances have been sized following Equation (1) to obtain four different voltage gains (5, 10, 100, and 600 V/V), considering that the LT1037ACN8 has a 60 MHz UGB stable for gains greater or equal to 5, obtaining respectively 40 kΩ, 90 kΩ, 990 kΩ, and 5.99 MΩ.

It is worth noting that the resulting feedback resistance values are implemented using series resistors because single commercially available resistors cannot be obtained. Afterward, the VGA was simulated through Multisim (Figure 5); the simulation results are

shown in Figure 6. The graphs in Figure 6 show the input and output signal waveforms, enabling evaluation of the design stage's gain and phase distortion.

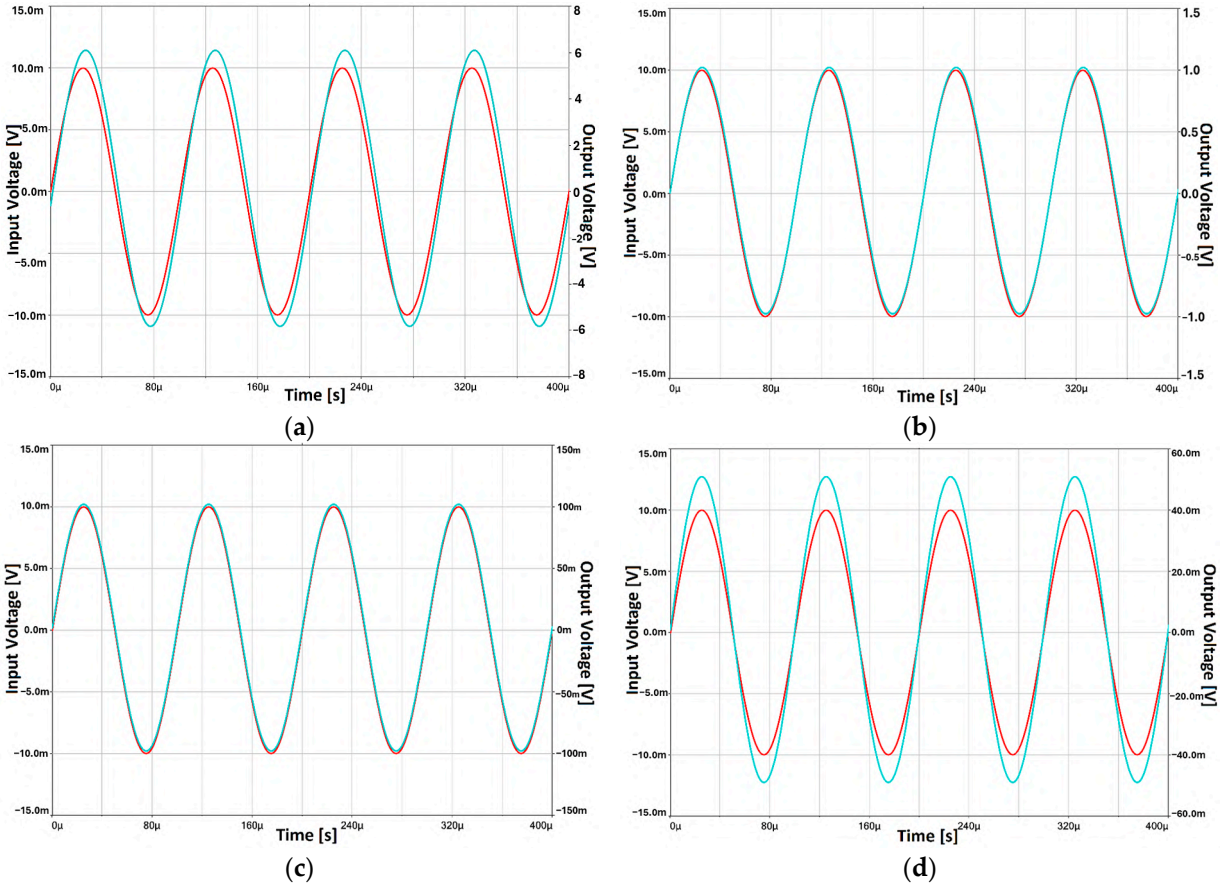


Figure 6. Simulations of VGA carried out with Multisim. The red trace is the input signal, and the blue one is the output signal for different set gains: (**a**) 600 V/V, (**b**) 100 V/V, (**c**) 10 V/V, and (**d**) 5 V/V.

Furthermore, a distortion analysis has been performed in Multisim to evaluate the THD (Total Harmonic Distortion) and SINAD (Signal-to-Noise and Distortion Ratio) of VGA (Table 1). The IEEE definition is used for the THD, whereas 10 harmonics and 1024 FFT points are considered [26]. In this application, the LT1037ACN8 op-amp employed for implementing the VGA is powered through a ±12 V dual supply.

Table 1. Distortion analysis results for the simulated VGA for different gains.

Gain	THD	SINAD
5 V/V	0.001% (<−100 dB)	92.612 dB
10 V/V	0.001% (<−100 dB)	91.836 dB
100 V/V	0.001% (<−100 dB)	91.884 dB
600 V/V	0.002% (−94.285 dB)	90.15 dB

2.2. Design of the Signal Conditioning Chain for "MODE 2"

The signal conditioning chain designed for "MODE 2" consists of a constant current source (namely the LT3092EST by Linear Technology Inc., Milpitas, CA, USA), which provides the constant current required from the IEPE sensor (2 mA ÷ 20 mA), and a level shifter based on the OPA27GP op-amp that transforms the IEPE sensor output to cover the 0 V ÷ +10 V range. The user can control the shift voltage V_{SHIFT} through a trimmer (Figure 7).

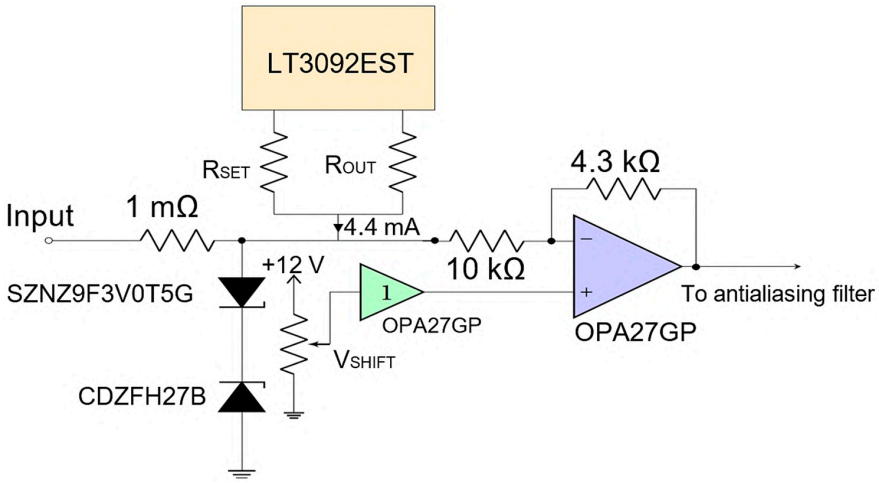


Figure 7. Functional block diagram of the signal conditioning chain for "MODE 2".

The LT3092EST module consists of a controllable 2-terminal current source, and two resistors, R_{SET} and R_{OUT}, are required to set the resulting output current between 0.5 and 200 mA. The current on the "SET" pin (I_{SET}) is fixed by a reference current of 10 µA. Thus, the output current I_{OUT} can be set in the following way:

$$V_{SET} = I_{SET} \times R_{SET} = 10\ \mu A \times R_{SET} \Rightarrow I_{OUT} = \frac{V_{SET}}{R_{OUT}} = 10\ \mu A\ \frac{R_{SET}}{R_{OUT}}, \quad (2)$$

In this application, the resistors R_{SET} and R_{OUT} are set to 120 kΩ and 270 Ω, respectively, thus resulting in an output current I_{OUT} equal to 4.4 mA.

This signal conditioning chain is preceded by a voltage limiter, which consists of a small resistor (of value equal to 1 mΩ) and two anti-series Zener diodes (namely the CDZFH27B and the SZNZ9F3V0T5G), whose Zener voltage absolute values $|V_{z,1}|$ and $|V_{z,2}|$ are equal to 27 V and 3 V, respectively. In this way, the input signal is limited in the range between $-(V_{z,2} + V_{\gamma,2})$ V and $+(V_{z,1} + V_{\gamma,1})$ V, where $V_{\gamma,1}$ and $V_{\gamma,2}$ are the forward bias voltages of the CDZFH27B and the SZNZ9F3V0T5G, respectively.

The level shifter implemented on the board is based on the OPA27GP op-amp. As described above, it transforms the output signal of the PCB 333B32 IEPE sensor to cover the range from 0 V to +10 V. The sensor's output is connected to a 10 kΩ resistor connected to the OPA27GP's inverting terminal (Figure 8). On the other hand, the shift voltage (V_{SHIFT}), provided by a voltage buffer also based on the OPA27GP, is applied to the positive terminal of the other level shifter's OPA27GP op-amp. The user can control the V_{SHIFT} through a trimmer. Moreover, the voltage buffer's OPA27GP op-amp has a dual-supply voltage (± 12 V), whereas the other is supplied from 0 V to +12 V.

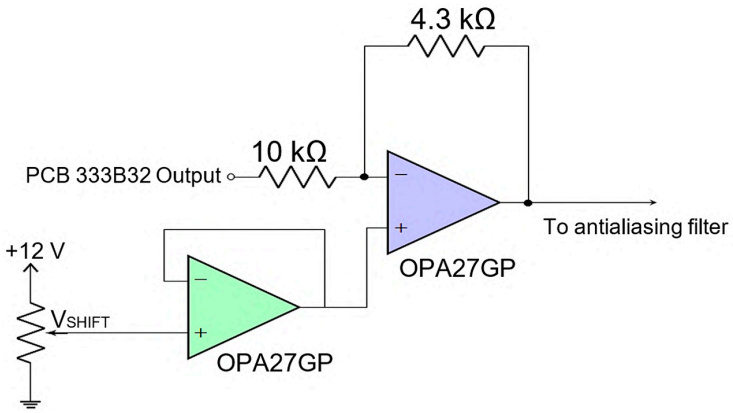


Figure 8. Circuit diagram of the designed level shifter.

The signal at the inverting terminal of the op-amp v_{IN} can be expressed as:

$$v_{IN} = Av_{in} + V_{IN}, \tag{3}$$

where v_{in} is the AC signal component featured by A amplitude, and V_{IN} is the DC component. Specifically, A is assumed to be 10 V_{pk}, and VIN is between 7 V and 12 V, following the PCB 333B32 IEPE sensor specifications. Therefore, a worst-case analysis was performed in the design of the level shifter, considering both the lower and upper limits of V_{IN}. Considering the superposition principle, v_{IN} is applied to an inverting configuration, and V_{SHIFT} is applied to a non-inverting configuration. In this way, the output of the level shifter can be written as follows:

$$v_{OUT} = -\frac{R_f}{R_{in}}(Av_{in} + V_{IN}) + \left(1 + \frac{R_f}{R_{in}}\right)V_{SHIFT}, \tag{4}$$

where R_f is the feedback resistance and R_{in} is the resistance at the inverting terminal of the op-amp. Thus, by letting $R_f/R_{in} \triangleq \alpha$ and separating the DC and the AC components of v_{OUT}, Equation (4) can be written as follows:

$$\begin{cases} V_{OUT} = -\alpha V_{IN} + (1+\alpha)V_{SHIFT} \\ v_{out} = -\alpha A v_{in} \end{cases}, \tag{5}$$

where V_{OUT} represents the DC component of v_{OUT} and v_{out} its AC component; hence, to obtain an input range from 0 V to +10 V, V_{OUT} must be set equal to 5 V and αA equal to 5 V_{pk}; thus, α is equal to 0.5. However, a more conservative value of α has been chosen to avoid saturation; therefore, α was set to 0.43. Considering both the upper and lower limits of $V_{IN,}$ i.e., 12 V and 7 V, respectively, the values of the shift voltage in each case, $V_{SHIFT,1}$ and $V_{SHIFT,2}$, are approximately 7.1 V and 5.6 V, respectively.

The level shifter has been simulated by Multisim (Figures 9 and 10); in the graphs of Figure 10, the red trace represents the input signal (V_{IN}), and the blue one is the level shifter output. Furthermore, a distortion analysis was performed in Multisim (Table 2); the IEEE definition is used for THD, considering 10 harmonics and 1024 FFT points.

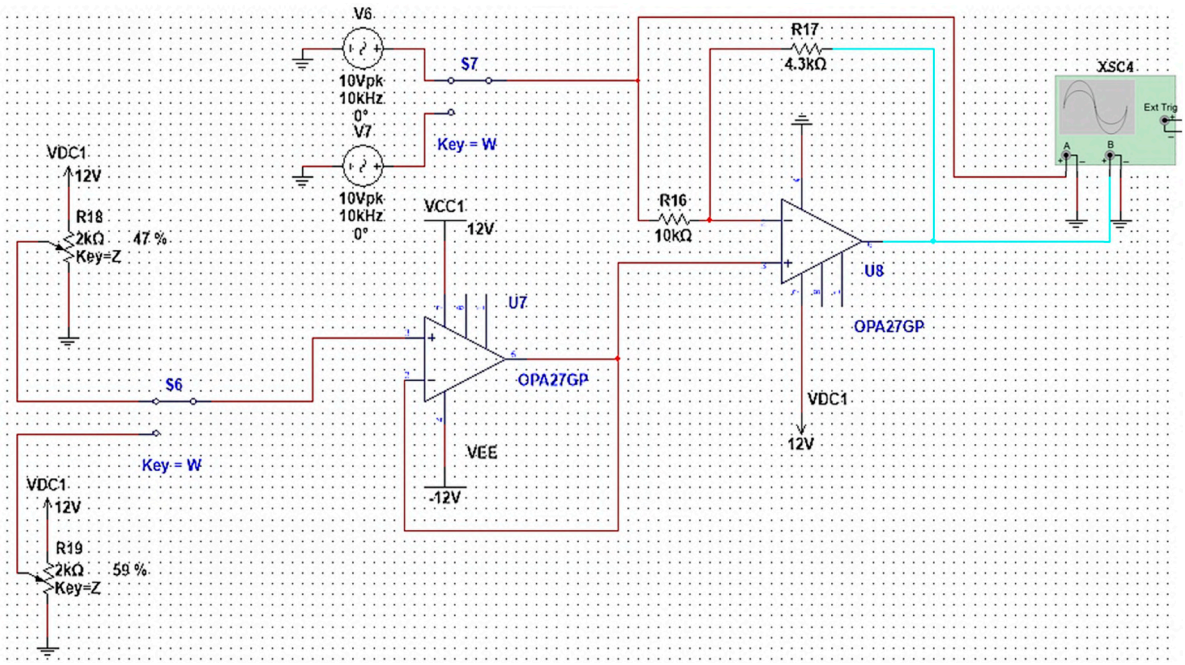


Figure 9. Multisim setup for the implemented level shifter. As stated before, two cases are considered for the DC component of the input signal, i.e., when V_{IN} is equal to 7.1 V and 12 V.

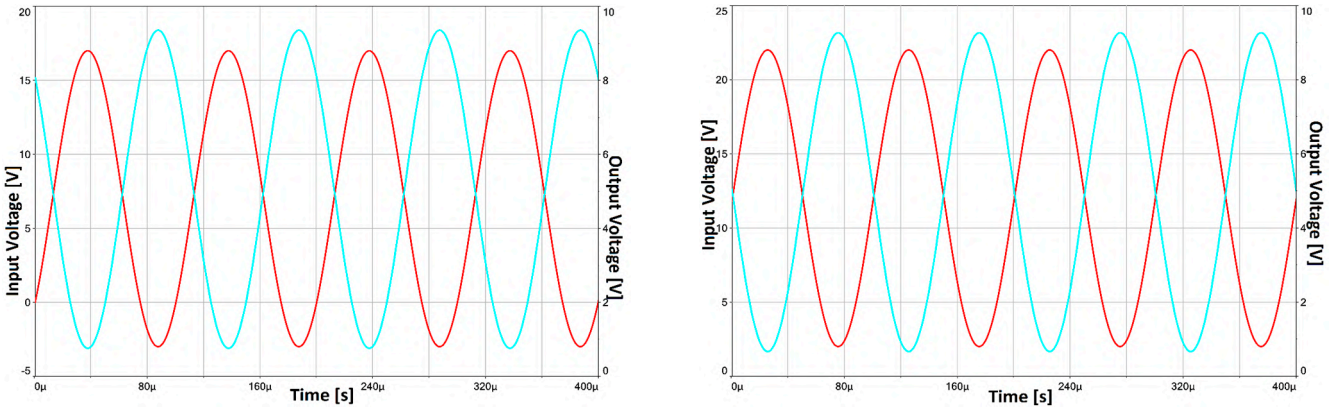


Figure 10. Results of the simulations for the proposed level shifter on Multisim (the red trace is the input signal, the light blue one is the output signal). (**a**) V_{IN} equal to 7.1 V and V_{SHIFT} equal to 5.6 V; (**b**) V_{IN} equal to 12 V and V_{SHIFT} equal to 7.1 V.

Table 2. Distortion analysis results for the level shifter for different input and shift voltages.

V_{IN}	V_{SHIFT}	THD	SINAD
7 V	5.6 V	0.001% (<−100 dB)	93.374 dB
12 V	7.1 V	0.005 (−86.773 dB)	85.778 dB

2.3. Antialiasing Filter Design

The employed antialiasing filter consists of a Sallen–Key (SK) low-pass filter (Figure 11). The cut-off frequency (f_{3dB}) and quality factor (Q) can be calculated as follows:

$$f_{3dB} = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \qquad Q = \frac{\sqrt{R_1R_2C_1C_2}}{C_2(R_1 + R_2)}$$

Specifically, the filter is designed to present unitary gain, a quality factor Q equal to $1/\sqrt{2}$, and a cut-off frequency f_{3dB} equal to 250 kHz. Hence, R_1, R_2, C_1, and C_2 present the following values: 12 kΩ, 7.5 kΩ, 100 pF, and 47 pF, respectively. The op-amp used in the design is the OPA27GP. The filter has been simulated through the Multisim software (version 14.1). The filter inputs represent the outputs of the two signal conditioning chains for either operating mode discussed above. Figures 12 and 13 show the filter's schematic on Multisim and the corresponding simulation results related to its transfer function.

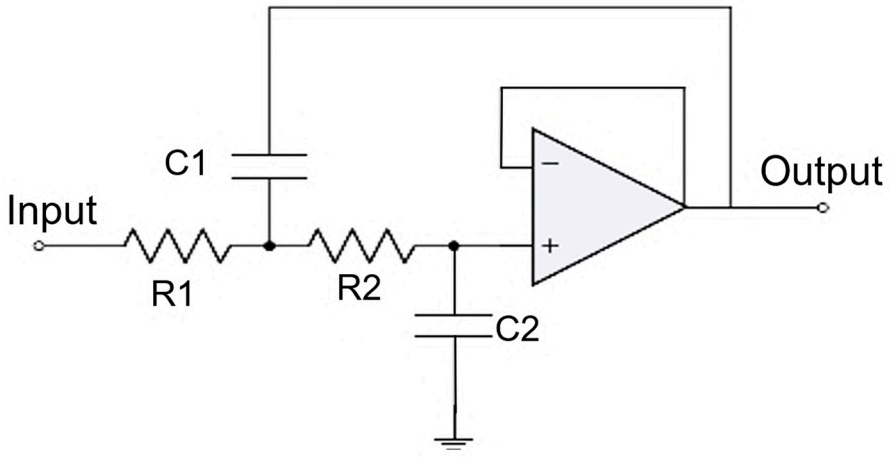


Figure 11. Circuit diagram for the low-pass SK filter.

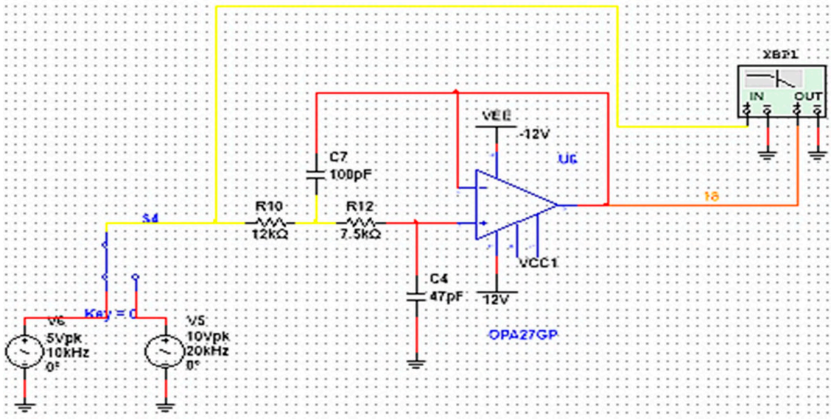


Figure 12. Multisim schematic for the implemented SK antialiasing filter.

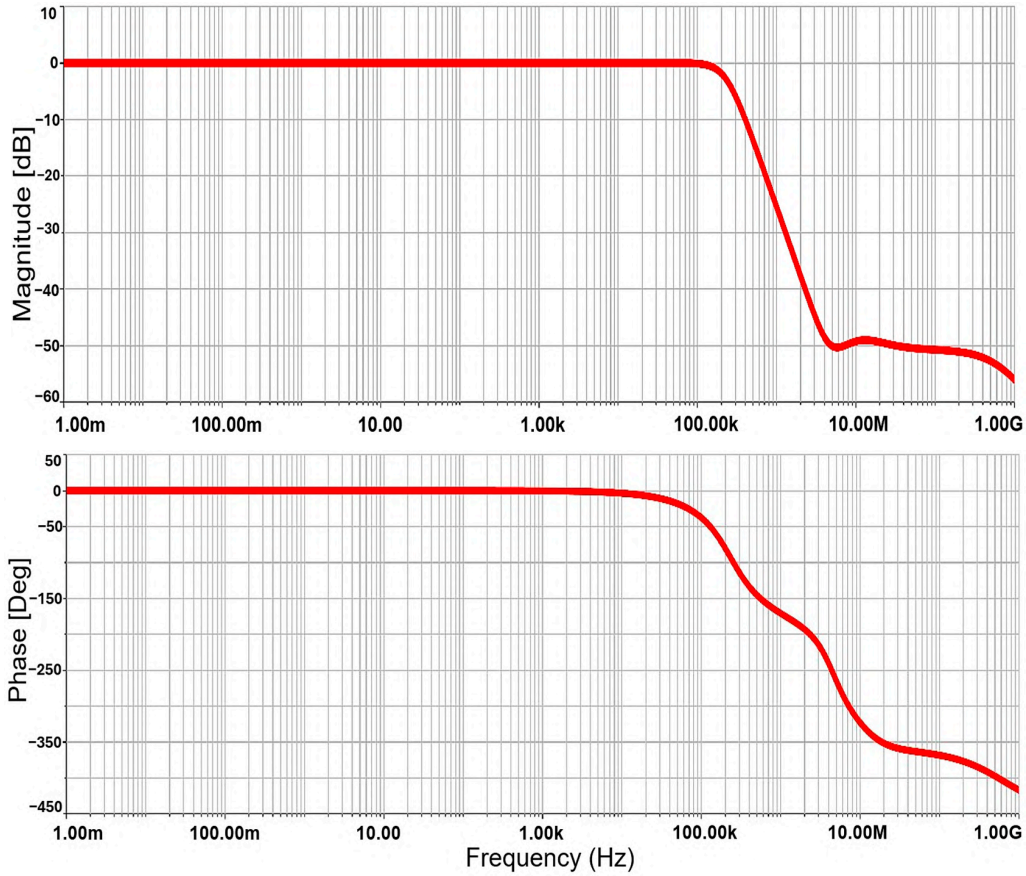


Figure 13. Bode plots for magnitude and phase responses of the simulated antialiasing filter. It is worth observing that these Bode plots are valid for both filter inputs, and the filter introduces two poles at approximately f_{3dB}, resulting in a −40 dB/decade attenuation.

Furthermore, THD analysis has been performed in Multisim, considering 10 harmonics and 1024 FFT points (Table 3). The filter is utilized for antialiasing purposes and to limit the bandwidth of the input signals, thus obtaining noise reduction and limitation.

Table 3. Distortion analysis results for the simulated filter considering the two modes of operation.

Mode of Operation	THD	SINAD
"MODE 1"	0.005% (−86.47 dB)	83.33 dB
"MODE 2"	0.002% (−94.285 dB)	85.787 dB

2.4. Acquisition and Processing Section of the Proposed DAQ for Vibration Analysis

The ADC chosen for each channel of the proposed DAQ is the AD7367-5 module (manufactured by Analog Devices Inc., Norwood, MA, USA) [27]. It consists of a 14-bit successive approximation ADC with a 500 kSPS maximum throughput and low power consumption, compatible with SPI, QSPI, and MICROWIRE communication interfaces. The AD7367-5′s integrated circuit includes two ADCs with a 2-channel analog multiplexer and a low-noise Sample and Hold circuit. The input range of this ADC is user-configurable in accordance with the logic levels of the "RANGE0" and "RANGE1" pins (Table 4).

Table 4. Combinations of the logic levels of the "RANGE0" and "RANGE1" pins of the AD7367-5 and the resulting input range.

"RANGE0"	"RANGE1"	Resulting Input Range
LOW	LOW	±10 V
LOW	HIGH	±5 V
HIGH	LOW	0 to +10 V
HIGH	HIGH	Do not program

The conversion begins on the falling edge of the "$\overline{\text{CONVST}}$" signal; "BUSY" must remain HIGH throughout the conversion process. If "$\overline{\text{CONVST}}$" is LOW when "BUSY" goes LOW, the circuitry shuts down, and the conversion process ends. The "BUSY" signal needs to remain HIGH for the whole duration of the conversion process, and the "$\overline{\text{CS}}$" signal must be set to LOW for bringing the data bus out of three-state. Nevertheless, the reading process needs 14 clock ("SCLK") cycles. The "D_{OUT}" lines return to three-state when "$\overline{\text{CS}}$" is set to HIGH.

If "$\overline{\text{CS}}$" is LOW for an additional 14 clock cycles, the data read from the other on-chip ADC can be obtained through the same "D_{OUT}" line. After 28 clock cycles, the "D_{OUT}" line is set to three-state when "$\overline{\text{CS}}$" is brought HIGH (it is worth observing that the line is not brought back to three-state on the 28th clock falling edge). If "$\overline{\text{CS}}$" is brought HIGH before this, then the "D_{OUT}" line is set to three-state at that point. Therefore, "$\overline{\text{CS}}$" needs to be brought to HIGH only when the reading process is complete since the bus does not automatically return to three-state if the reading of the dual result is completed. When a data transfer is completed and both "D_{OUTA}" and "D_{OUTB}" have been set to three-state, then the AD7367-5 can initiate another conversion process by bringing "$\overline{\text{CONVST}}$" LOW again when a time interval t_{QUIET} (which must be 50 ns minimum) has passed.

The microcontroller selected to acquire and process data from A/D converters is the STM32F401CC (manufactured by STMicroelectronics S.p.A., Geneva, Switzerland) [28]. This microcontroller was chosen because of its computing capabilities and wide set of integrated peripherals and interfaces. Table 5 reports the STM32F401CC's main parameters.

Table 5. STM32F401CC's main parameters.

SMT32F401CC Main Parameters	
Processor	32-bit ARM® Cortex®-M4 equipped with an FPU
Flash Memory	256 kB
Data Memory	64 kB
Clock frequency	16 MHz internal RC oscillator, external 4–26 MHz clock source (25 MHz integrated), PLL for clock frequency up to 84 MHz
I^2C interfaces	3
USART interfaces	3
SPI interfaces	Up to 4
SDIO interfaces	1
USB 2.0 interfaces	1
DMAs	2 with 8 streams each
Power dissipation	128 µA/MHz in run mode, 42 µA in stop mode, 10 µA in deep power mode, 2.4 µA in standby mode

In this application, the MCU is powered through a 5 V supply. Moreover, a stand-alone microcontroller section was deployed in the design of the proposed acquisition board. In detail, a Blackpill prototyping board based on the STM32F401CC microcontroller was employed and integrated into the proposed DAQ board. In particular, the DAQ board includes two 20 × 1 female headers placed according to the Blackpill's footprint, allowing for an easy and reliable connection with the prototyping board. This way, the MCU can be eventually changed, if necessary, to upgrade the system in the future.

The LXX-0581 is a Micro SD reader module connected with the MCU through a file system and an SPI interface. The MCU then completes the file system to be read and written to a MicroSD card [29]. The HC-06 is a class-2 Bluetooth serial module that enables wireless serial communication between the microcontroller and other Bluetooth-compatible devices [30]. Regarding the specific application, it wirelessly transmits the acquired data to an external computer. The HC-06 can be configured either as a master or slave modality. In the first one, the module can search and select the device to be connected. On the contrary, in slave mode, the module can be searched by the host device but cannot be actively searched. The module supports supply voltages in the range of 3.3 V ÷ 5 V. In this application, the HC-06 is used as a slave device and is fed to a 3.3 V voltage supply.

2.5. PCB Design of the Proposed DAQ Board

This section describes the design of the printed circuit board (PCB) of the proposed acquisition system for vibrational analysis, which is designed through Autodesk EAGLE CAD software version 9.4.2. In the designed board, two JST connectors are utilized to provide the power supplies (+15 V and +26 V, respectively), a 2 × 1 male header to provide the external trigger signal, and four BNC connectors to provide the inputs of each channel; specifically, two BNC connectors correspond to each channel, one for each operation mode. In addition, the board includes 22 µF by-pass ceramic SMD (Surface Mount Device) capacitors, used for removing any high-frequency components on the power supply line.

Moreover, the JST connectors are equipped with red and blue LEDs to indicate the power supplies applied to the +15 V and +26 V connectors, respectively. The power supply section includes the LM2940T-12.0, ICL7660AIBA, BD50FA1FP3-ZTL, and BD33FA1FP3-ZTL cascaded voltage regulators, all equipped with their respective by-pass capacitors. In addition, a diode is connected between the "VOUT" and "CAP-" pins of the ICL7660AIBA to prevent an eventual latch-up.

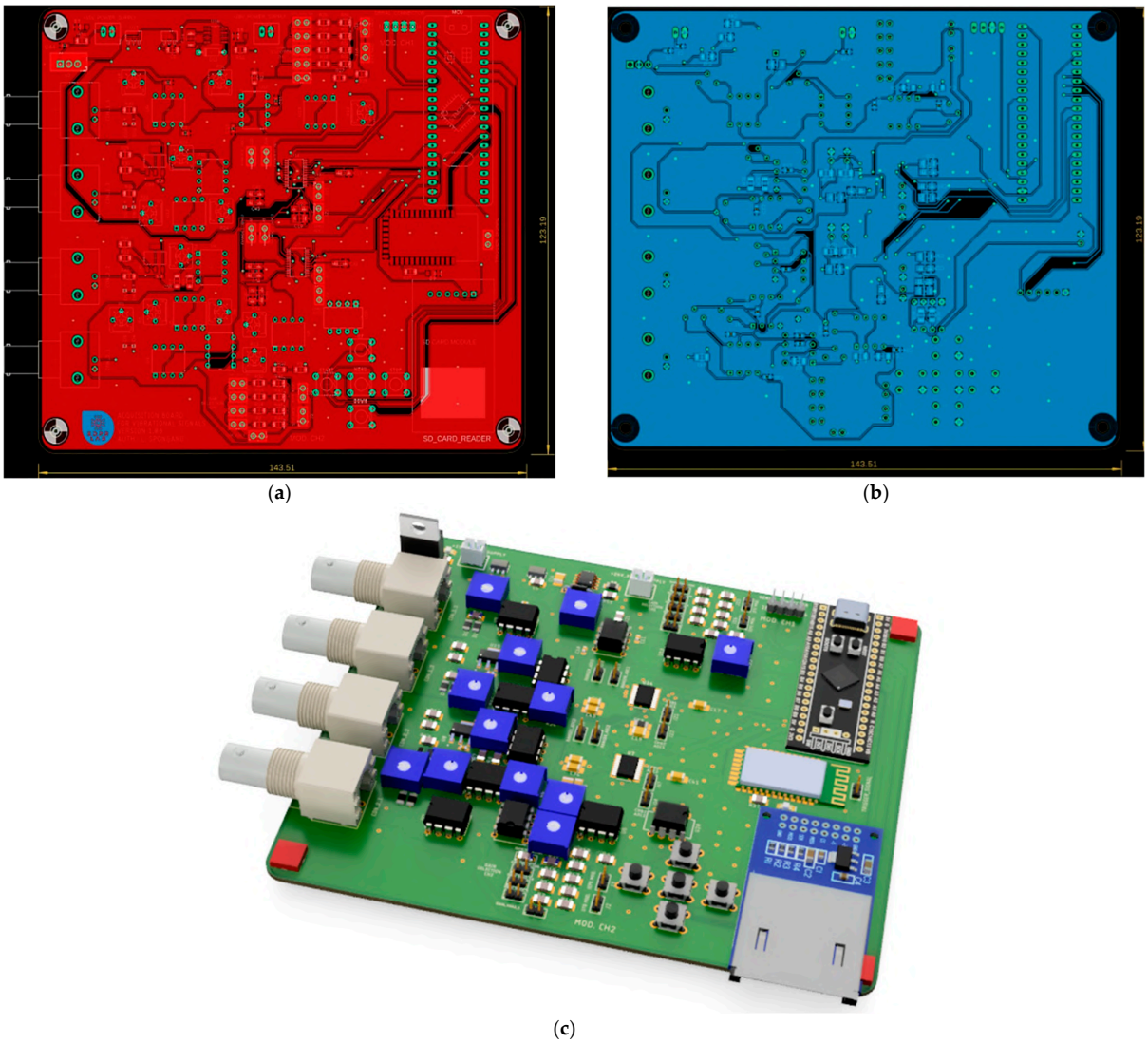
Each BNC connector is connected to its respective voltage limiter. Concerning the analog portion of "MODE 1", each channel includes the OPA27GP op-amps used for the realization of the voltage buffers, equipped with by-pass capacitors on the voltage supplies and a 10 kΩ trimmer for voltage offset reduction, and the LT1037ACN8 op-amps used for the realization of the VGAs. These last comprise 2 × 1 male headers to select the desired gain through jumpers on the feedback loops, by-pass capacitors on the power supply lines, and a 10 kΩ trimmer to reduce voltage offset. Furthermore, each VGA includes a 10 kΩ SMD resistor connected to its negative terminal and the feedback SMD resistors used to obtain the desired gain.

Concerning the analog sections of "MODE 2", they both include the LT3092EST current generator, equipped with SMD resistances to set the output current, and by-pass capacitors on the power supply lines. Also, these sections include two OPA27GPs for implementing the level shifters, each including their respective by-pass capacitors on their power supply lines. The 10 kΩ variable resistors are used to trim their voltage offset. In addition, two 10 kΩ trimmer resistances are used to regulate V_{SHIFT}. Moreover, other SMD resistors are used to set each level shifter's gain. Each analog portion includes another OPA27GP op-amp for implementing the antialiasing filters, each equipped with two 2 × 1 male headers to select the mode of operation via a jumper. Each OPA27GP op-amp comprises by-pass capacitors on the power supply lines and a potentiometer for trimming the voltage offset. Furthermore, each filter employs the respective SMD resistors and ceramic capacitors.

Every acquisition channel includes its ADC, each including its corresponding electrolytic tantalum SMD capacitors, two 2 × 1 male in series with 10 kΩ SMD resistors to set the logic levels on the "RANGE0" and "RANGE1" pins of each ADC via jumpers. Moreover, two 2 × 1 male headers are connected to the B-channels of each ADC for using those channels by properly setting the logic level on the "ADDR" pin via firmware.

Finally, the digital section includes two 20 × 1 female headers placed according to the Blackpill footprint, five 6 mm × 6 mm buttons, and a 4 × 1 male header to interface the MCU with the HC-06 Bluetooth module. Also, the digital section includes an LM393N comparator equipped with two 10 kΩ SMD resistors to create a voltage divider and a 2 × 1 male header to provide an external trigger signal. Lastly, a 6 × 1 female header is used to interface the LXX-0581 SD card reader with the MCU through an independent SPI interface. The Bill of Material (BOM) needed for assembling the DAQ board has been attached to the Supplementary Materials (File S1).

Afterward, the employed devices' footprints are placed on the top and bottom layers to reduce the PCB dimensions. Moreover, two ground planes were included, both in the top and bottom layers, to reduce the EMI (ElectroMagnetic Interference) of the board, thus improving its robustness. Also, they provide an easy way to connect each component to the ground, inserting additional via holes between these two ground planes where required. The resulting dimensions of the designed PCB are 143.51 mm in width and 123.19 mm in height (Figure 14).



(**a**) (**b**)

(**c**)

Figure 14. (**a**) Top, (**b**) bottom, and (**c**) 3D views of the designed acquisition board.

3. DAQ Board Prototype to Test the Proposed Architecture

A system prototype for firmware development and testing the correct operation of single sections before realizing the final DAQ's PCB has been developed using evaluation boards and stand-alone components. The prototype consists of:

- Blackpill SMT32F401CC board.
- 2 × AD7606 ADC evaluation boards.
- W25Q64FV flash memory.
- LXX-0581 SD card reader.

The inputs of the ADCs are provided by a function generator (i.e., the FY3200s, manufactured by Feeltech Inc., Zhengzhou, China). The ADCs and the W25Q64FV flash memory are connected to the same SPI bus, whereas the SD card reader is connected to an independent SPI bus. It is worth observing that the Blackpill board supports integration with an additional flash memory, which can be mounted on the bottom layer of the Blackpill board. The evaluation boards based on the AD7606 were chosen because AD7606's serial communication protocol is similar to that of AD7367-5, and evaluation boards based on AD7367-5 have not been found on the market. Figure 15 shows the prototype schematic; Figure 16 displays the corresponding setup, including a STlink v2 debugger for programming and debugging the firmware on the Blackpill board and a USB-to-serial converter for exchanging control messages, in addition to the system's prototype.

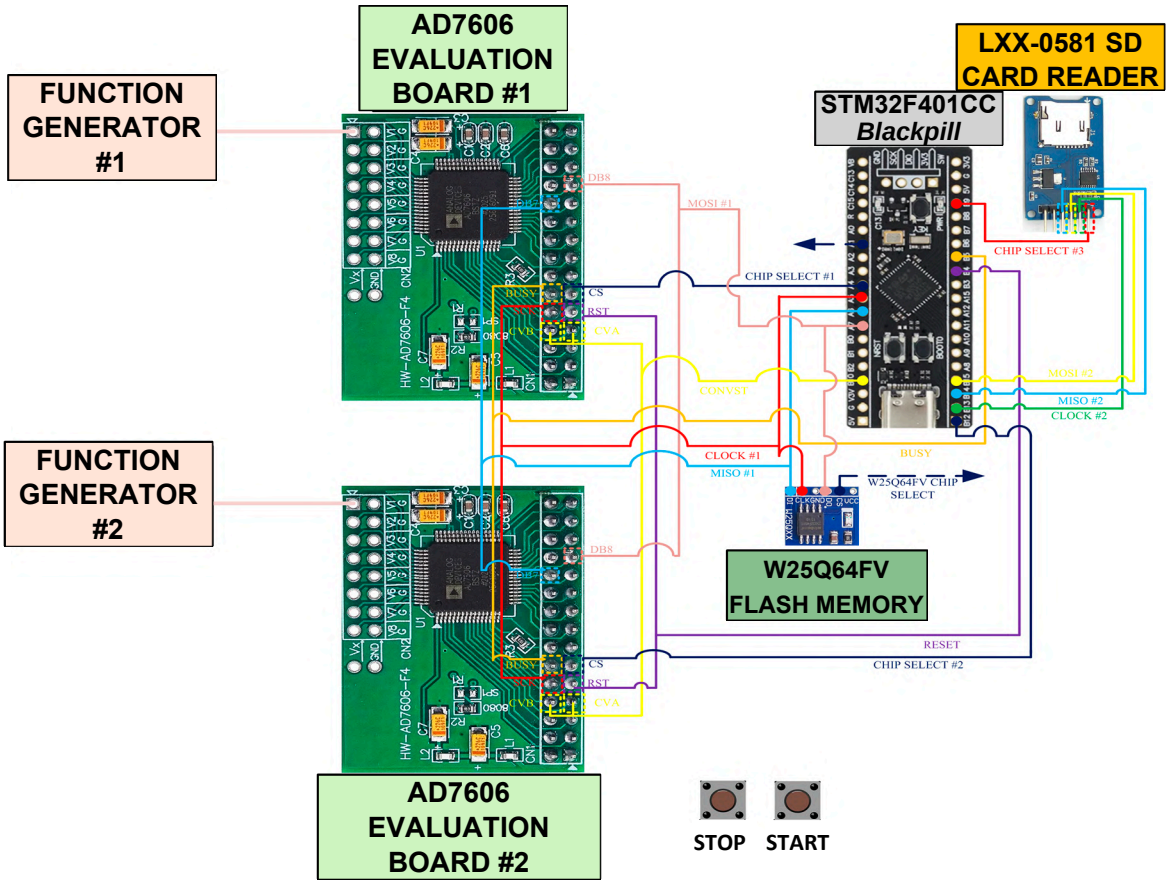


Figure 15. DAQ prototype's schematic.

The W25Q64FV is a 64-megabit serial flash memory device compatible with the SPI, Dual/Quad I/O SPI, and QPI communication protocols. It operates on a single power supply voltage between 2.7 and 3.6 V and supports clock frequencies up to 104 MHz [31].

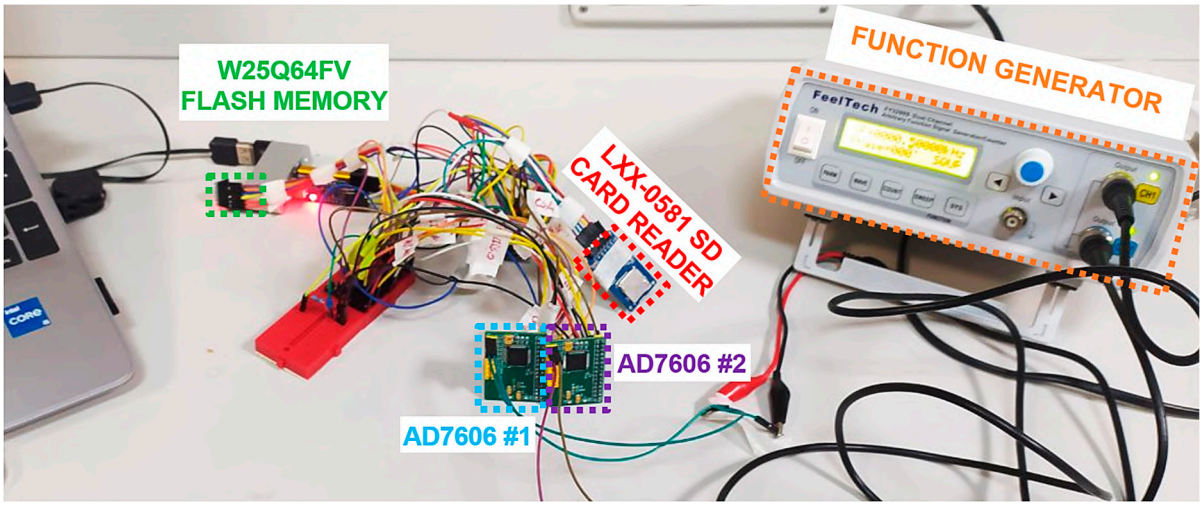


Figure 16. Setup employed for the DAQ prototype.

The AD7606 (manufactured by Analog Devices Inc., Norwood, MA, USA) is a 16-bit ADC capable of simultaneous sampling on 8 channels [32]. The IC includes circuitry for analog clamp protection, a second-order low-pass antialiasing filter, a SH circuit for each channel, a 16-bit successive-approximation ADC, a digital filter, a 2.5 V buffered voltage reference, and serial and parallel interfaces. The AD7606 can read bipolar input signals with ± 10 V or ± 5 V input ranges selectable through the logic level of the "RANGE" pin.

The AD7606 has three user-selectable communication modes: a parallel interface, a high-speed serial interface, and a parallel byte interface. The communication mode can be chosen by using the "$\overline{\text{PAR}}$/SER/BYTE SEL" and "DB15" pins. In this work, the serial mode is used ("$\overline{\text{PAR}}$/SER/BYTE SEL" is HIGH, whereas "DB15" is LOW) since, as previously mentioned, it is similar to the communication modality supported by the AD7367-5.

Furthermore, on the evaluation board, the selection of the serial mode is achieved by leaving the "R2" slot floating and placing a 10 kΩ resistor in the "R1" slot. In this mode, the "$\overline{\text{CS}}$" and "SCLK" signals are used to transfer data from the AD7606 using the SPI communication protocol. The device has two serial output pins, "$D_{OUT}A$" and "$D_{OUT}B$". The user can read the data using one or both output lines. The results of the conversion process from channels "V1" to "V4" appear on the "$D_{OUT}A$" pin, whereas the conversion results from channels "V5" to "V8" appear on the "$D_{OUT}B$" pin.

The falling edge of "$\overline{\text{CS}}$" takes the data output lines out of three-state, and the conversion result's MSB is clocked out. Then, the "SCLK" rising edge clocks all subsequent data bits onto the serial data outputs. The "$\overline{\text{CS}}$" line can be maintained LOW for the serial read operation; otherwise, it can be pulsed to frame each channel read in 16 SCLK cycles. Data can also be clocked out using only one output line; 128 "SCLK" cycles are required. These "SCLK" cycles can either be framed by one "$\overline{\text{CS}}$" signal or each group of 16 "SCLK" cycles can be individually framed by the "$\overline{\text{CS}}$" signal. The limit of using only one output data line is that the throughput rate is reduced if reading occurs after the conversion process.

Firmware Development of the Proposed DAQ Board

This section analyzes the firmware developed in the STM32Cube IDE (Integrated Development Environment) for the system prototype based on the AD7606 ADC. The firmware does the following tasks sequentially:

- The variables, the buffers to temporarily store the data bytes and the timestamp bytes, the GPIOs, and the communication interfaces are initialized.
- The DMA (Direct Memory Access) is initialized.
- The AD7606s are reset.
- The filesystem is mounted on the SD card; two CSV files are created afterward.
- The W25Q64FV is reset by performing a whole-chip erase.

Then, for each cycle of the infinite loop, the firmware does the following:

- It waits until the "START" button is pressed.
- Subsequently, until the "STOP" button is pressed or the maximum allowed number of pages is reached, an inner "*for*" loop of 128 iterations is initialized to allow the data acquired from the two AD7606s and the corresponding timestamp to be stored into the respective buffers. This operation is performed because the pages of the W25Q64FV can be programmed in blocks of 256 bytes. Furthermore, each transfer requires 2 bytes per channel and 4 bytes per timestamp. The data from the two AD7606s is acquired using the DMA and stored byte by byte, whereas each timestamp is decomposed into 4 bytes. Hence, four *uint8_t* buffers store the data and the timestamps. Once the inner for loop is complete, the raw data bytes of the first channel are stored on the ith page of the external flash memory, whereas those of the second channel are on the (i + 1)th page. Moreover, the timestamps are stored in the (i + 2)th and (i + 3)th pages. Then, the page count is incremented by 4.
- Once the "STOP" button is pressed or the page count has reached the maximum number of pages, a "*for*" loop is initialized; this loop is iterated until the page counter reaches the page number used in the previous step. In this "*for*" loop:
    - If the current page counter modulo 4 equals 0, the data from the first AD7606 is read from the corresponding W25Q64FV page, is then composed into the respective buffer, and then the FFT is performed on the collected samples.
    - If the current page counter modulo 4 equals 1, the data from the second AD7606 is retrieved from the corresponding W25Q64FV page and is then composed into its respective buffer. Subsequently, the FFT is performed on the collected samples. The frequency axis and the results of the FFT of each channel are then written into the second CSV file on the SD card.
    - If the current page counter modulo 4 equals 2, timestamps #0 to #63 are read from the respective W25Q64FV page, recomposed, and stored into the first half of the timestamp buffer. The timestamps and the data from the two AD7606s are then written into the first CSV file on the SD card.
    - If the current page counter modulo 4 equals 2, timestamps #64 to #127 are read from the corresponding W25Q64FV page, recomposed, and stored into the second half of the timestamp buffer. The timestamps and the data from the two AD7606s are then written into the first CSV file on the SD card.
- Once the operations in the for loop are concluded, the two CSV files are closed, and two new CSV files are created on the SD.

Figure 17 depicts the high-level flowchart describing the code's tasks, and Figure 18 depicts how the W25Q64FV pages are organized to store the raw data bytes from the two channels and the timestamp bytes. In detail, the method for acquiring data from AD7606 ADCs, called "*readRAW*", accepts two pointers to memory locations where acquired data are stored. Subsequently, the CNVST pin is brought LOW to start the conversion on both AD7606s since it is connected in parallel to both devices (Figure 15). Subsequentially, CONVST is set to HIGH, and a while loop is then initialized, waiting until the BUSY pin is LOW (Figure 19a). Then, the CS pin of the first AD7606 is set to LOW, and the microcontroller reads the 16-bit sample on the SPI bus through DMA (Figure 19a). Afterward, the CS of the first AD7606 is brought back to HIGH; the same steps are also performed for the second AD7606, considering the proper CS. After, the sample data from the two ADCs are stored in two 256-byte buffers, as well as the 32-bit timestamps are decomposed into 4-byte and stored in a further buffer (512-byte). After the buffer filling, they are poured into four flash memory pages (Figure 18). The function used to write a page of the W25Q64FV flash memory, called "*w25qWritePage*", takes the page pointer and the page number as its parameters, then initializes an array with the following bytes: *W25Q_WRITE_ENABLE* (0x06), 0x00, 0x00, and 0x00 (Figure 19b). Afterward, the block protection functionality is disabled, the memory CS is set to LOW, and the *W25Q_WRITE_ENABLE* byte is transmitted

through the SPI bus. The CS is brought back to HIGH; then, the remaining array elements are updated so that the first element is *W25Q_PAGE_PROGRAM* (0x02), and the remaining three bytes represent the page number. The next step consists of setting the chip select to LOW, transmitting the array and page pointer, and then returning the chip select to HIGH (Figure 19b). The function waits until the W25Q64FV flash memory is ready again; then, the first element of the array is set to *W25Q_WRITE_DISABLE* (0x04), and CS is lowered. Thus, the first element of the array is transmitted via SPI, and the CS is brought back to HIGH. Afterward, the W25Q64FV's block protection functionality is enabled using the *w25qSetBlockProtect*(0x0F) instruction.

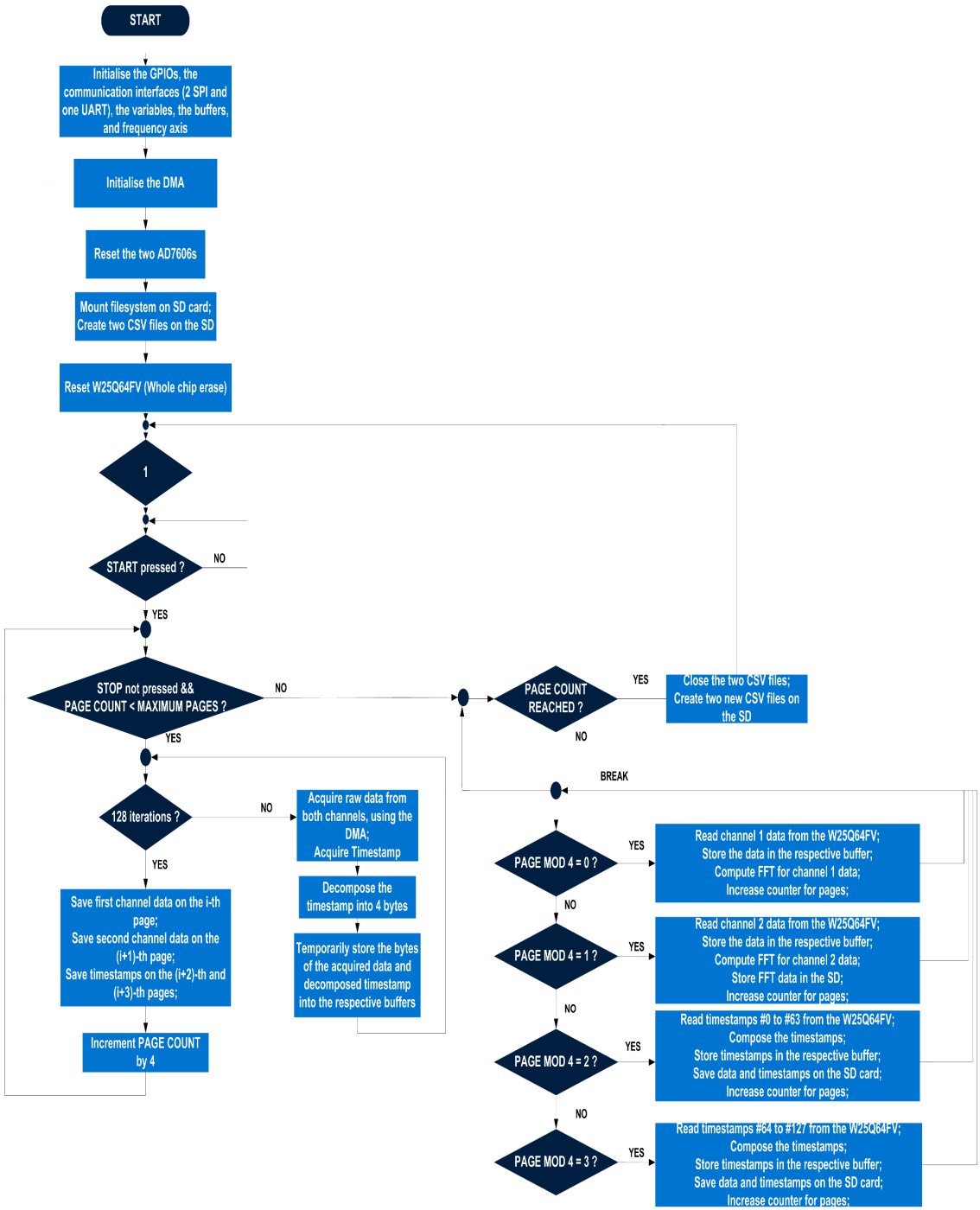


Figure 17. High-level flowchart for the firmware developed for the prototype board based on the AD7606.

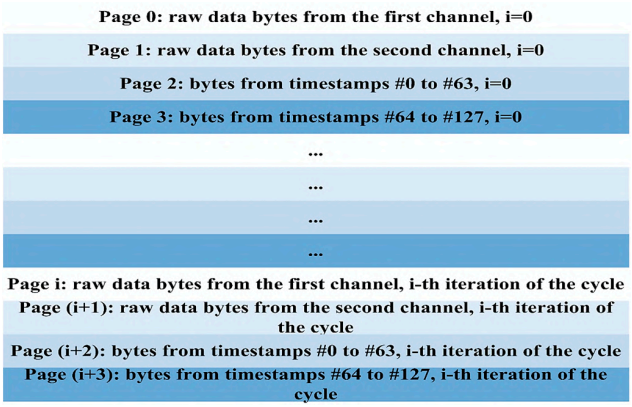


Figure 18. Organization of the W25Q64FV pages.

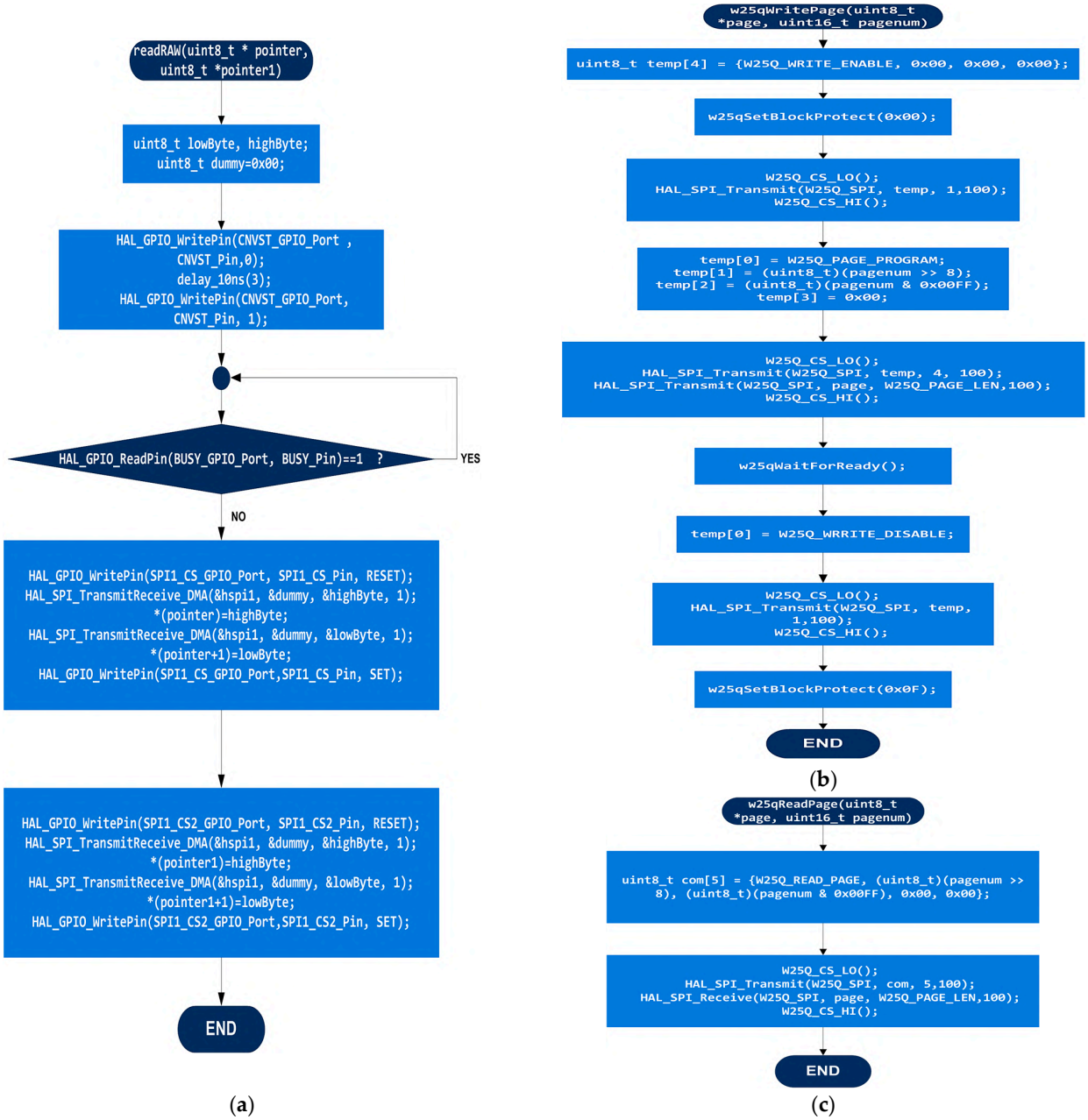


Figure 19. Flowchart of the following methods: (**a**) *readRAW()*, (**b**) *w25qWritePage()*, and (**c**) *w25qReadPage()*.

After the "STOP" button is pushed or the memory page's counter reaches the memory limit, a loop is initialized over the flash memory pages to recover data from flash memory and copy it into the SD card. The function to read a page from flash memory (*w25ReadPage*) accepts the page pointer and the page number as parameters. Then, an array of five elements is declared and initialized with the following bytes: *W25Q_READ_PAGE* (0x0B), 2 bytes representing the page, and 2 bytes set to 0x00 (Figure 19c). Afterward, the CS is set to LOW, and the array above is transmitted. After that, the content of the required W25Q64FV page is received, and the memory CS is brought back to HIGH (Figure 19c).

Afterwards, a loop is initialized (with counterPage iterations). A variable m is declared first in this loop and set to the loop counter (*k*) modulo 4. Then, a switch statement is performed on *m*; depending on the value of *m*, different code blocks are executed:

- For each case, the kth page of the W25Q64FV is read, and its content is stored in the buffer by using the *w25ReadPage()* method.
- If *m* equals 0, the FFT is initialized, and its magnitude is computed on a 128-element buffer representing the samples of the first channel (Figure 20).
- If *m* equals 1, the FFT is initialized, and its magnitude is computed on a 128-element buffer representing the samples of the second channel. After the FFT computation, another for loop is initialized, in which the frequency axis and the results of the FFT computation on the first and second AD7606 ADCs are stored in a CSV file (Figure 20).
- If *m* equals 2, a loop is initialized to recover the timestamps of the first 64 samples (Figure 20).
- Lastly, if *m* equals 3, a loop constituted by 64 iterations (with z as index) is initialized to recover the timestamps of the last 64 samples of both channels. After the timestamp recomposition, the two 128-element buffers are multiplied for the ADC quantization step; the results are saved in a separate CSV file (Figure 20).

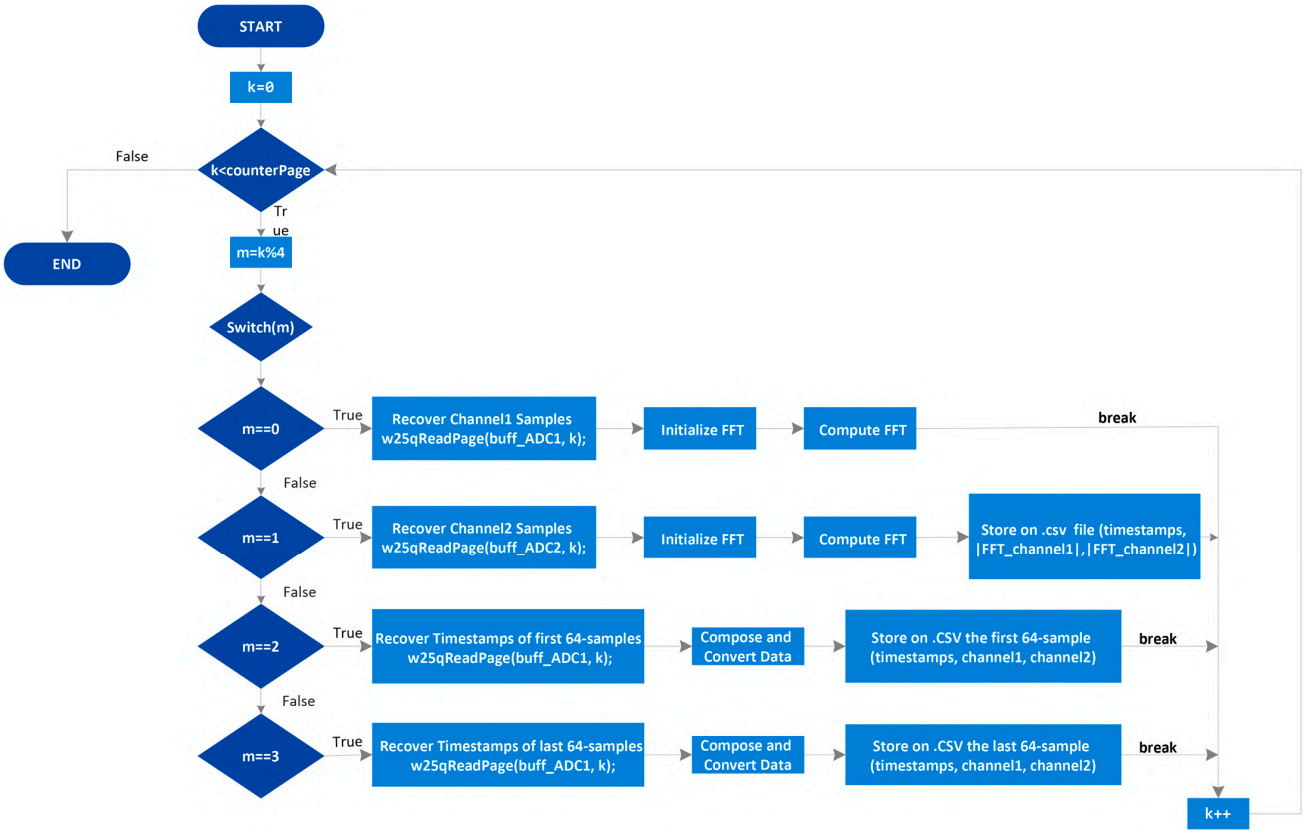


Figure 20. Flowchart related to the data recovery from flash memory, FFT calculation, and data storage into CSV files on the SD card.

For further details regarding the developed firmware, the DAQ board code was added as Supplementary Materials (File S2).

4. Tests Performed on the DAQ Prototype

The following section presents the results of the experimental tests conducted on the prototype based on the AD7606 ADC to evaluate its performances and functionalities. The first test consists of calculating its sampling frequency. According to the AD7606′s datasheet, the sampling frequency is defined as the inverse of the time between two consecutive "CONVST" pulses, which in the context of this work corresponds to the time interval between two consecutive acquisitions.

At first, the preliminary tests used to measure the sampling frequency were performed with a modified version of the firmware, designed to employ only a single AD7606 ADC. In this scenario, the measured time interval between two consecutive acquisitions was 45 µs, corresponding to a sampling frequency of 22.2 kHz. Nevertheless, if both AD7606s are utilized, the measured time interval between two consecutive acquisitions was 80 µs, corresponding to a sampling frequency of 12.5 kHz. This sampling frequency allows for the acquisition of signals whose bandwidth is up to 5 kHz without being distorted by aliasing. Since the reference IEPE sensor provides a signal with a bandwidth of up to 3 kHz, the developed DAQ system prototype also complies with the corresponding Nyquist frequency (6 kHz) when two channels are acquired [25].

The following tests are executed to verify the correctness of the acquired signals. Thus, the second test involves the acquisition of an AC signal from the first AD7606 and a DC voltage from the second one. The setup for this test is the following: the first AD7606 is connected to a function generator, the other to the "VBAT" pin of the Blackpill, which provides a DC voltage of 1.87 V. In this test, the function generator provides a square wave of peak-to-peak amplitude equal to 1 V, DC offset equal to 2 V, and frequency equal to 500 Hz. The CSV file provided by the DAQ system prototype was plotted by MATLAB r2021a; the waveforms related to the two channels are shown in Figure 21, where the blue and orange traces represent the signals applied on channels 1 and 2, respectively. The acquired waveforms display some noise. However, the underlying trend of the signals remains distinguishable. Nevertheless, despite the noise, the essential features of the acquired signals are retained and can still be analyzed.

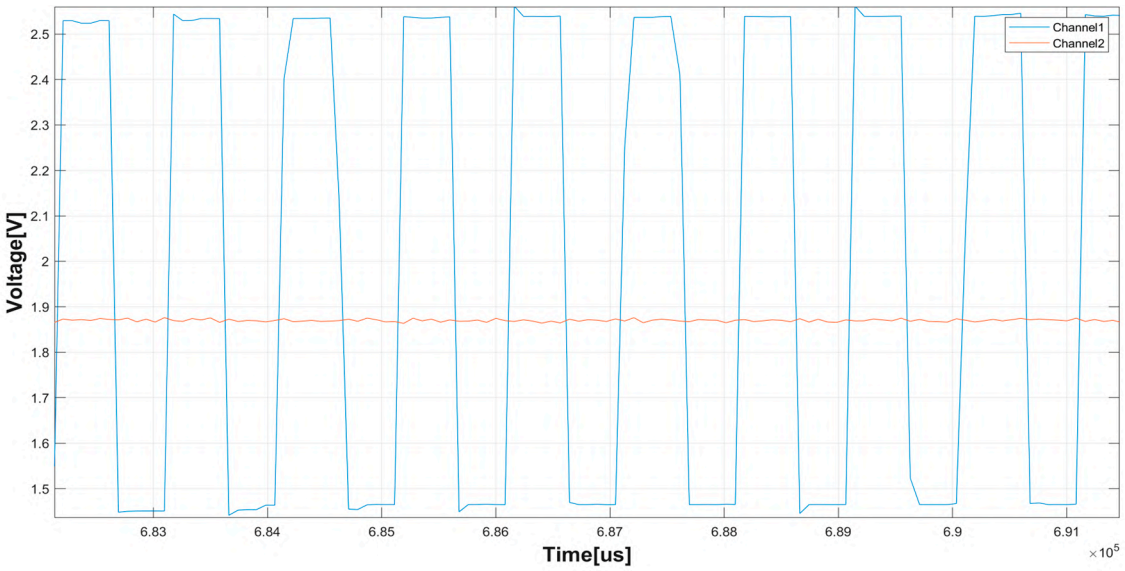


Figure 21. Waveforms acquired by the developed DAQ system prototype on channel 1 (500 Hz square wave, blue trace) and channel 2 (1.87 V DC voltage, orange trace).

The third test is similar to the second one, as it involves the acquisition of an AC signal from the first AD7606 and a DC voltage from the second. In particular, the function generator connected to the first AD7606 yields a square wave with the following parameters: frequency 1 kHz, 1 V peak-to-peak amplitude, and DC offset 2 V. The second AD7606 is connected to the "VBAT" pin of the MCU, which provides a 1.87 V DC voltage.

The waveforms acquired by the DAQ's prototype are shown in Figure 22, where the blue and orange traces represent the signals applied on channels 1 and 2, respectively. The measured period of the square wave is equal to 1047 µs, corresponding to a frequency of 955.1 Hz, close to the nominal frequency of 1 kHz.

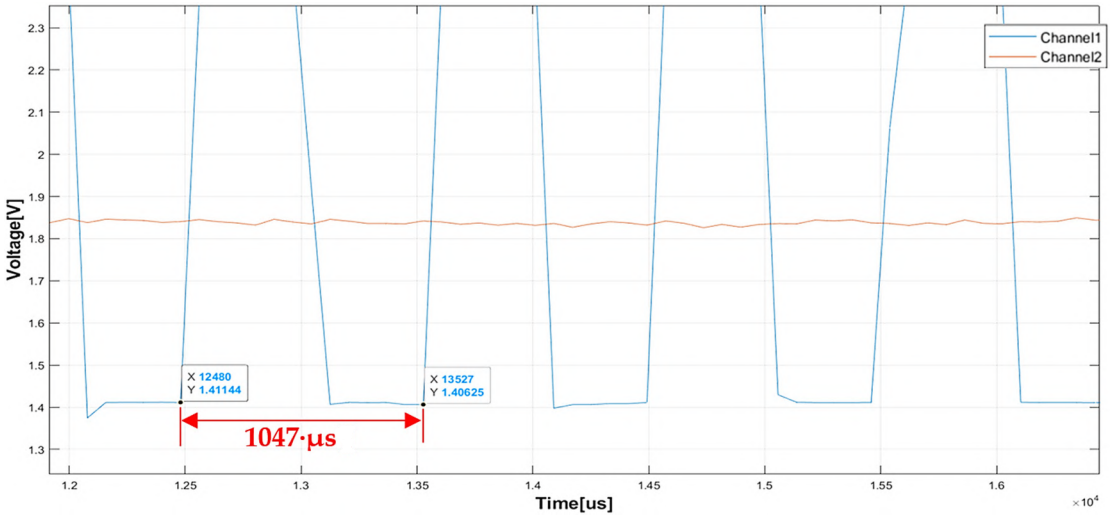


Figure 22. Detailed view of the waveforms acquired by the developed DAQ system prototype on channels 1 (1 kHz square wave, blue trace) and 2 (1.87 V DC voltage, orange trace), with the period of the square wave emphasized (1.047 ms).

The fourth test involves the acquisition of two AC signals. The test setup consists of a function generator that provides a square wave to the first AD7606 and a sine wave to the second one. The parameters of the square wave are the same as the previous test, whereas the parameters of the sine wave are as follows: the frequency is equal to 1 kHz, the peak-to-peak amplitude is equal to 1 V, and 2 V is the DC offset.

The waveforms related to the two channels are shown in Figure 23, where the blue and orange traces represent the signals applied on channels 1 and 2, respectively.

As shown in Figure 23, the two signals are in phase, as expected, since the "CONVST" pins of both AD7606s are connected in parallel, thus allowing the conversions to be started simultaneously. For the last test, two AC signals are acquired from the two AD7606s, and then the FFT is computed on both the acquired signals. In this test, the function generator provides two square waves of amplitude (peak-to-peak) equal to 1 V and a DC offset equal to 2 V, connected to the AD7606s. The square wave provided to the first AD7606 has a 1 kHz frequency, whereas the other has a 500 Hz frequency.

Figure 24a,b plots the modulus of the FFT calculated by the microcontroller on the signals applied on the two channels of the DAQ prototype. As shown in Figure 24a, for the signal applied on channel 1 (i.e., 1 kHz square wave), the harmonic peaks occur at the frequencies of 937.5 Hz, 2906.5 Hz, and 4875 Hz; these results are close to the peak frequencies of the ideal spectrum, namely 1000 Hz (fundamental frequency, f_0), 3000 Hz ($3f_0$), and 5000 Hz ($5f_0$). Figure 24b depicts the bilateral FFT for the signal applied on channel 2 (i.e., 500 Hz square wave); as can be observed, the harmonic peaks exist at the frequencies of 468.75 Hz, 1500 Hz, and 2437.5 Hz; these values are close to the peak frequencies of the ideal spectrum, namely f_0 (500 Hz), $3f_0$ (1500 Hz), and $5f_0$ (2500 Hz).

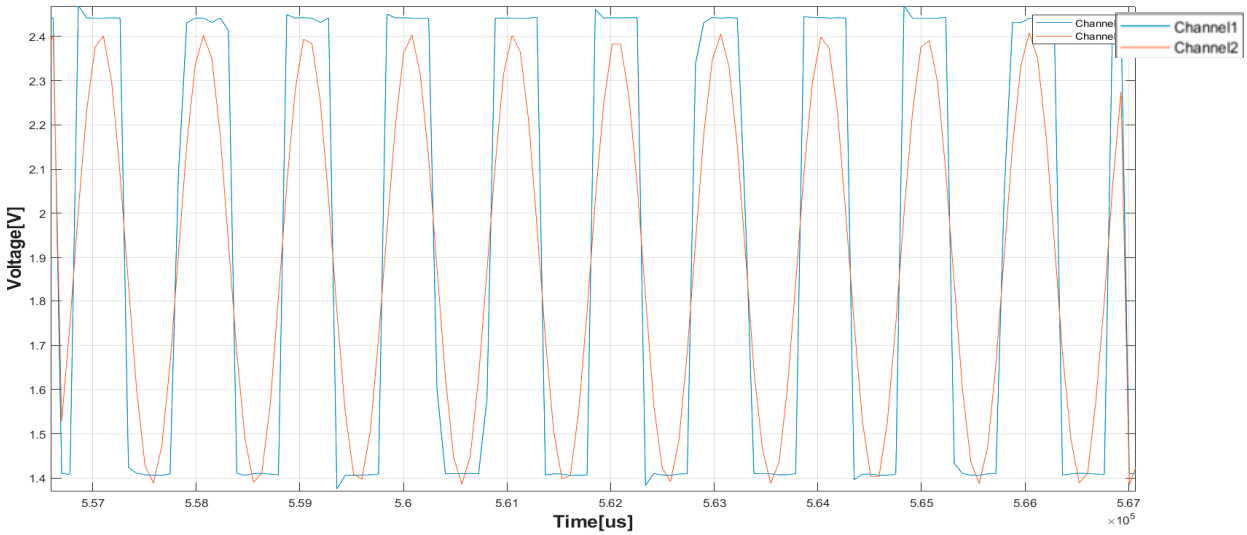


Figure 23. The developed DAQ system prototype acquired waveforms on channel 1 (1 kHz square wave, blue trace) and channel 2 (1 kHz sine wave, orange trace).

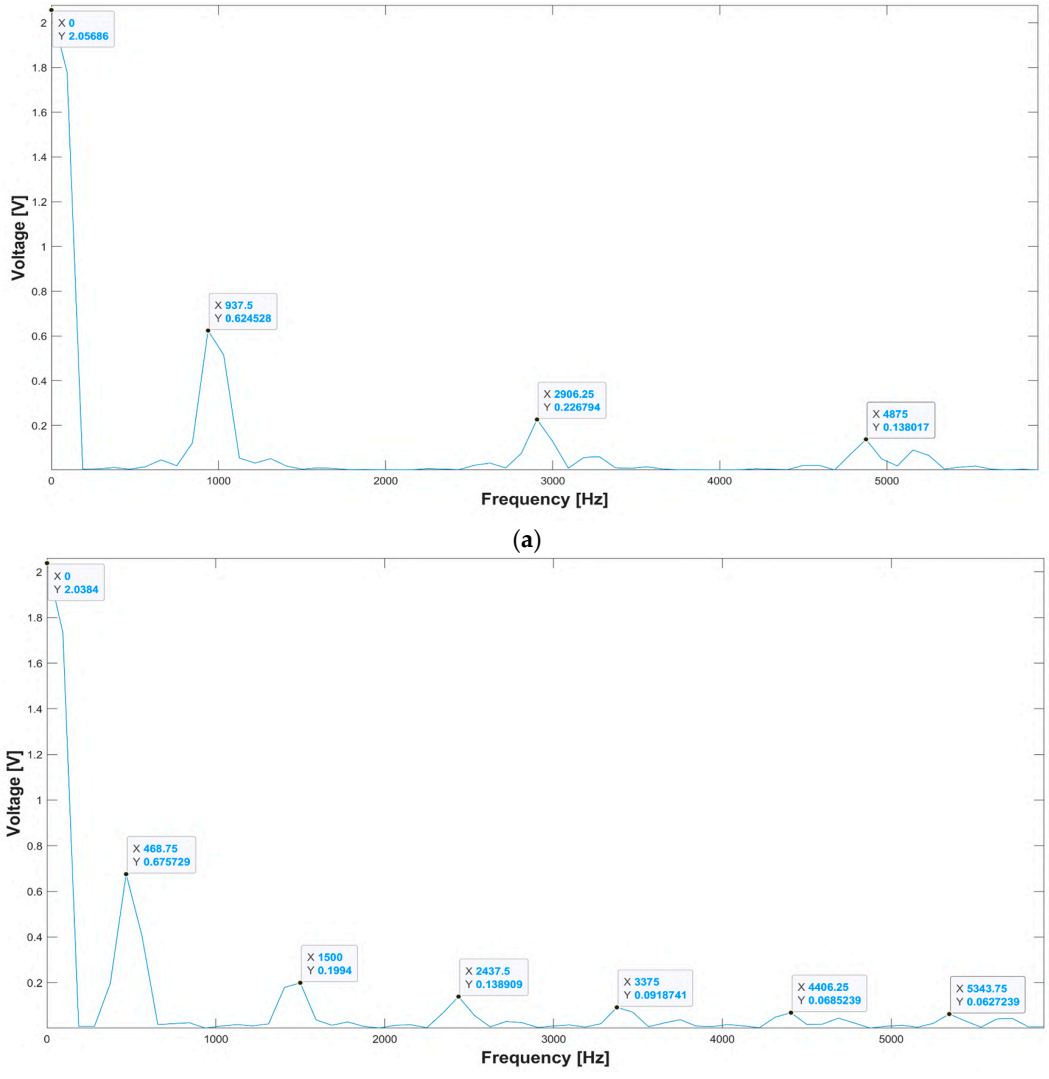


Figure 24. Fifth test: (**a**) single-side band FFT for channel 1 (1 kHz square wave) and (**b**) channel 2 (500 Hz square wave) signals (in the makers, X is the frequency and Y is the harmonic amplitude).

The last tests involved the FFT computation of vibration signals generated by the bearings' rotation induced through an AC motor and acquired from an IEPE sensor; therefore, the supposed scenario could fall within the monitoring of generic machinery driven by an AC motor. The input signals, related to the acceleration components along the x and y axes, feature a dominant oscillation at 1 kHz frequency with 1.5–2 V amplitude values, along with secondary components with lower amplitude. The signals consist of the, and each component was properly digitized, converted into the corresponding voltage, and conditioned to fit the input range of the AD7606 ADC (i.e., ±5 V). Subsequently, the resulting signals were converted into .csv format and reproduced using the EDU33210 function generator (manufactured by Keysight Inc., Santa Rosa, CA, USA). The function generator outputs were then connected to the two channels of the AD7606-based DAQ prototype. The resulting signals were acquired with a sampling frequency equal to 12.5 kHz, and the onboard 128-point FFT was calculated using. Figure 25 displays the vibrational waveforms, while Figure 26 shows the 128-point FFTs calculated onboard by the DAQ's prototype. The comparison between the input signal and the one reconstructed at the output of the DAQ (Figure 25) demonstrated that the latter maintained all the features of the original one, highlighting the DAQ's prototype capability of acquiring vibration signals. As shown in Figure 26, the spectra of the acquired vibrational signals both present their dominant frequency around 1 kHz, reaching 1.83 and 1.18 V for the vibrational signal along the *x*-axis and the *y*-axis, respectively.

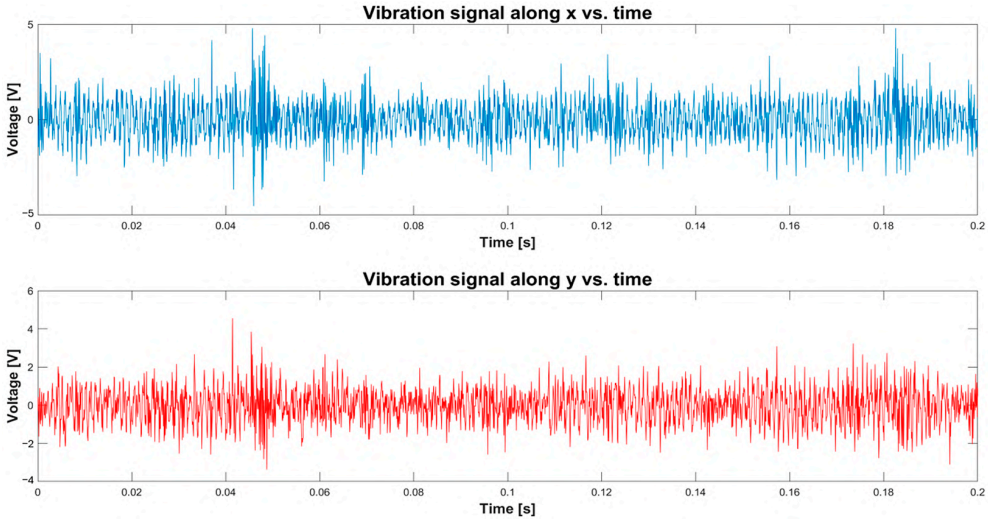


Figure 25. Vibrational signals acquired by the DAQ board: *x*-axis (blue trace) and *y*-axis (red) signals.

Furthermore, to analyze the capability of the DAQ prototype to capture low-frequency signals, a vibrational signal with a 100 Hz main frequency was considered. The 100 Hz frequency value was chosen since it is typical of industrial machinery, like turbines, milling machines, industrial lathes, high-speed grinders, etc.; however, the system operation was verified for a vibration system with a frequency content ranging up to kHz, demonstrating the proper operation of the proposed DAQ system. The input signal was generated by a shaking table and then conditioned, digitalized, and reproduced in the same way described before. The signal thus reproduced by the function generator was applied to channel 1 of the DAQ board's prototype; Figure 27 shows the waveform acquired at 1 kHz sampling frequency, programmed by firmware as a function of the input signal frequency. In addition, Figure 28 displays the vibration signal's spectrum computed through the 128-point onboard FFT. Comparing the original signal with the acquired one, the latter kept the characteristics of the input vibration signal, making the DAQ board's prototype suitable for acquiring low-frequency vibration signals. As reported in Figure 28, the vibration signal FFT's modulus presents its peak approximately at 100 Hz, reaching an amplitude of 4.38 V. However, the FFT resolution could be improved by increasing the FFT length at the expense of longer processing time, which we have already tested experimentally.

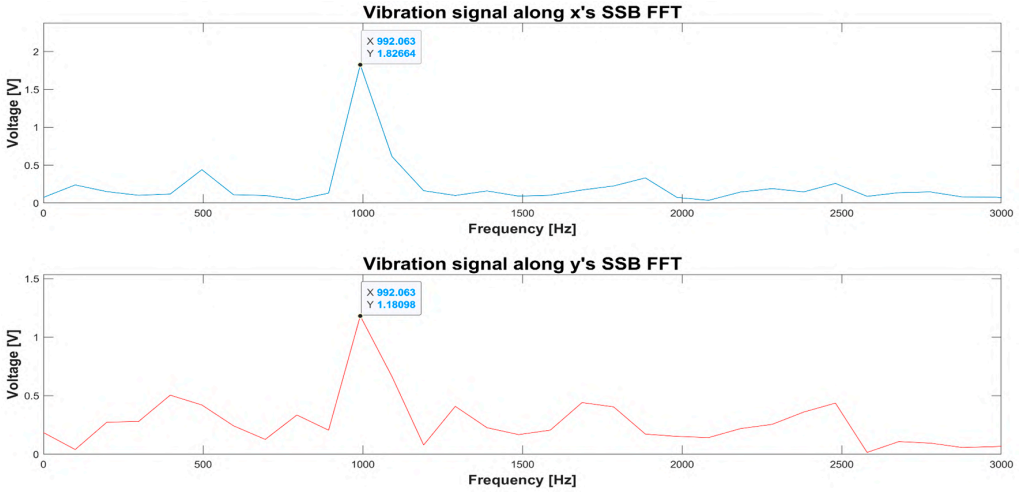


Figure 26. SSB FFT of the vibrational signals acquired by the DAQ board: *x*-axis (blue trace) and *y*-axis (red trace) signals (in the makers, X represents the frequency and Y represents the harmonic component amplitude).

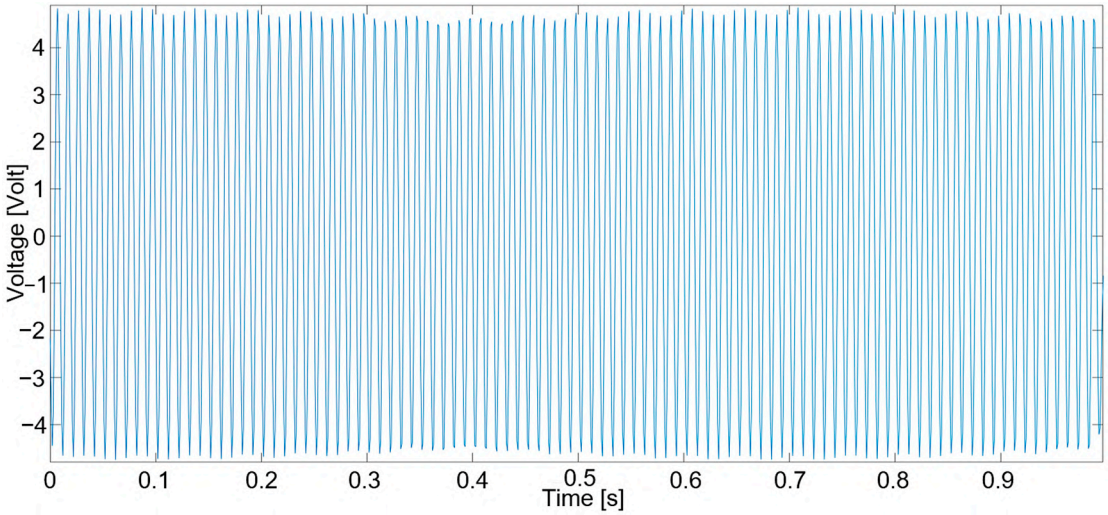


Figure 27. Low-frequency sinusoidal vibrational signal acquired by the DAQ prototype.

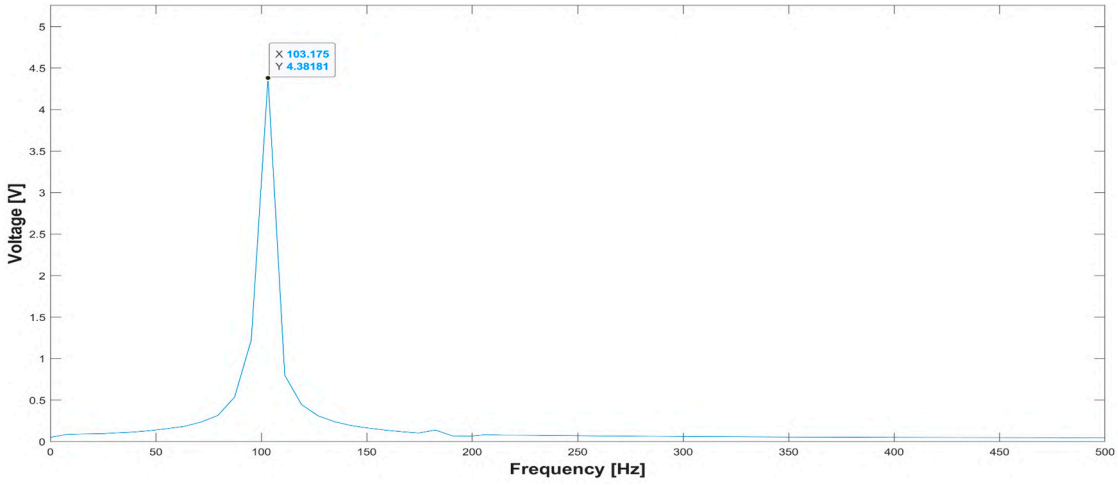


Figure 28. SSB FFT of the low-frequency vibrational signals acquired by the DAQ board prototype (in the makers, X represents the frequency and Y represents the harmonic component amplitude).

5. Discussions

Based on the hardware design for the acquisition board for vibration signals and the firmware developed for the prototype that employs the AD7606, the specifications of the proposed DAQ board are summarized in Table 6 as follows: As evident, the presented DAQ board shows high versatility, enabling the setting of the parameters of the acquisition stage (VGA gains, ADC input range) to adapt them to the features of the input signal. Furthermore, the DAQ sampling frequency can be regulated by firmware, controlling the frequency with which the microcontroller queries the ADCs. Moreover, as previously discussed, each channel can be set in two different modalities according to the board used to acquire signals from IEPE sensors ("MODE 1") or a generic voltage source ("MODE 2"), enabling the use of the board for different applications.

Table 6. Specifications of the developed DAQ board.

Specification	Condition	Value
N° of channels	Two independent channels, each with a dedicated ADC with a user-selectable input range.	2
ADC input range	Selectable manually by jumpers	± 5 V ± 10 V
ADC resolution	-	14 bit
Sampling frequency	Selectable by firmware	Maximum values: 22.2 kHz (one channel), 12.5 kHz (both channels)
VGA gains	Selectable manually by jumpers	1, 5, 10, 100, 600
IEPE sensor operating range	-	±50 g
IEPE sensor bandwidth	-	3 kHz
Acceleration resolution	-	6.1 mg
Conditioning section THD	MODE 1 MODE 2	0.012% (−76.83 dB) 0.008% (−85.05 dB)
Conditioning section SINAD	MODE 1 MODE 2	72.500 dB 75.288 dB
N° of point for onboard FFT computation	Selectable by firmware	128, 256, 512, 1024
Connectivity	-	Bluetooth

The conditioning sections related to the two modalities of the DAQ board obtained excellent performance in terms of THD and SINAD. Finally, the DAQ board performs a 128-point FFT on the data acquired by the ADCs related to the two channels, avoiding post-processing of the data after the acquisition. However, the length of the FFT calculated by the microcontroller can be increased by acting on the firmware (e.g., point numbers 256, 512, 1024), enhancing the spectrum resolution. In addition, the performance of the STM32F401CC microcontroller in carrying out the FFT over the acquired signals is analyzed, determining the FFT computation time as a function of the FFT length (Table 7). In detail, the tests were performed by turning compiler optimization on (-Ofast) and off (-O0) in a fast modality, a setting offered by STM32CubeIDE, enabling it to speed up the firmware execution and reduce the memory occupation. From Table 7, measured FFT computation times are suitable for onboard post-processing of acquired vibrational data, promptly providing the processed data to the user without needing post-processing on an external device. This observation, combined with the low cost of the proposed DAQ board, further confirms the qualities of the designed system for accurate vibration monitoring. As evident,

compiler optimization provides some benefits in terms of computation time, offering a 12% mean reduction.

Table 7. FFT processing time as a function of FFT length with/without compiler optimization.

	FFT Computation Time [µs]	
FFT Lenght	**Without Compiler Optimization**	**With Compiler Optimization**
128	215	198
256	454	417
512	1158	976
1024	2576	1924

Tables 8 and 9 below present a comparative analysis between the proposed DAQ board for vibration analysis and those found in the existing literature, from the point of view of the ADC number of bits, sampling frequency, number of acquisition channels, range of used inertial sensors, resolution, and availability of external memory support. Tables 8 and 9 suggest that the proposed DAQ board features excellent specifications, representing a preferable solution compared to other ones reported in the scientific literature since it provides a good trade-off in terms of ADC number of bits, sampling frequency, hardware complexity, and costs. Furthermore, the proposed system features an optimal trade-off between operating range and resolution on acquired measurements; indeed, there are solutions featuring higher resolution but on a narrow conversion range, limiting the analysis interval [1–3,11,18]. There are solutions featured by higher resolution, sampling frequency, employing more performant, and thus expensive components [3,15].

Table 8. Comparative analysis between the proposed DAQ board and those found in the literature regarding resolution, sampling frequency, number of channels, and input VGA availability.

Work	ADC Bit Number	Sampling Frequency	Number of Channels	Input VGA Availability	Inertial Sensor Operating Range	Resolution
C. R. Soto-Ocampo et al. [3]	16-bit	35 kHz using all channels	4	No	±20 g	0.61 mg
S. M. Shyni et al. [12]	8-bit	N.A. (*)	1	No	N.A.	N.A.
R. S. Mathad et al. [13]	N.A. (*)	N.A. (*)	N.A. (*)	Yes	N.A.	N.A.
A. Villarroel et al. [14]	12-bit	20 kHz	1	No	±500 g	0.24 g
H. Guo et al. [15]	16-bit	200 kHz	8	No	N.A.	N.A.
S. Hu et al. [16]	16-bit	N.A. (*)	1	No	±250 g	7.6 mg
G. Gopalakrishna et al. [11]	10-bit	1 kHz	1	No	±3 g	5.8 mg
I.A. Jamil et al. [1]	10-bit	N.A. (*)	1	No	±3 g	5.8 mg
K. Gürkan et al. [2].	12-bit	100 Hz	1	No	±8 g	3.9 mg
Y.Gorbounov et al. [18]	12-bit	Up to 1 MHz	Up to 17	No	±3 g	1.4 mg
Proposed DAQ Board	14-bit	22.2 kHz (one channel), 12.5 kHz (both channels)	2	Yes	±50 g	6.1 mg

(*) N.A.—not available.

Table 9. Comparative analysis between the proposed DAQ board for vibration analysis and those found in the existing literature regarding employed sensor type, presence of input filers, support for external memory, a dedicated ADC for each channel, and onboard FFT computation.

Work	Employed Sensor	Input Filtering	Support for External Memory	Dedicated ADC for Each Channel	Onboard FFT Computation
C. R. Soto-Ocampo et al. [3]	Generic piezoelectric accelerometer	No	Yes	No	No
S. M. Shyni et al. [12]	Generic piezoelectric accelerometer	Yes	No	Single channel	No
R. S. Mathad et al. [13]	Generic piezoelectric accelerometer	Yes	No	N.A. (*)	N.A. (*)
A. Villarroel et al. [14]	IEPE accelerometer	Yes	Yes	Single channel	No
H. Guo et al. [15]	IEPE accelerometer	Yes	Yes	No	No
S. Hu et al. [16]	IEPE accelerometer	Yes	No	Single channel	No
G. K. Gopalakrishna et al. [11]	MEMS accelerometer	No	No	Single channel	No
I.A. Jamil et al. [1]	MEMS accelerometer	No	No	Single channel	No
K. Gürkan et al. [2].	MEMS accelerometer	No	No	Single channel	No
Y.Gorbounov et al. [18]	MEMS accelerometer	N.A. (*)	No	No	No
Proposed DAQ Board	IEPE accelerometer, compatible with other sensor types	Yes	Yes	Yes	Yes

(*) N.A.—not available.

The developed DAQ board is compatible with IEPE sensors and other sensor types, has two independent acquisition channels available, and includes an antialiasing low-pass filter, an input VGA, and a dedicated ADC for each channel. Moreover, the board is completely programmable, thus making it flexible for several industrial scenarios. Also, the onboard FFT is an advantage, avoiding post-processing and promptly providing the user with essential information for modal analysis. Another strength of the proposed DAQ is the reduced cost; indeed, the estimated cost of the DAQ board is EUR 400–500, much lower than commercially available solutions, which can exceed EUR 3500–4000. Commercial solutions, usually based on Digital Signal Processors (DSP) and Field Programmable Gate Arrays (FPGA), can offer better performance in terms of resolution and processing time; nevertheless, the presented DAQ board provides an excellent balance between performance, available functionalities, flexibility, and costs.

Finally, the developed DAQ board is intended to perform real-time acquisition and processing of vibrational signals. However, considering the FFT processing times (Table 7) and that a single-core microcontroller is used, vibration signals with a frequency in the order of tens of Hz can be acquired without information loss. Otherwise, the FFT calculation involves information loss for signals with a higher frequency. As a future development, the acquisition/processing processes could be implemented by a dual-core platform (e.g., STM32H747, manufactured by *STMicroelectronics*), entrusting the data acquisition and processing/transmission phases to different cores.

6. Conclusions

The presented paper proposes the design and test of an effective and low-cost DAQ for acquiring and processing signals from IEPE sensors and generic signal sources, obtaining a useful tool for vibrational analysis studies. The developed DAQ board comprises a 14-bit resolution and encompasses two independent acquisition channels, each equipped with an independent ADC. Both channels can be utilized with general-purpose or IEPE sensor inputs, and they include an input VGA with a configurable gain between 1 and 600 V/V. Before the ADC, each channel integrates an antialiasing Sallen–Key low-pass filter. The DAQ board lies on an STM32F401CC microcontroller, which acquires, processes, and stores data provided by ADCs; in detail, a proper firmware was deployed, implementing a batch acquisition strategy, iteratively storing vibrational data into a buffer flash memory, and transferring it

into the mass memory, represented by the micro-SD card. A DAQ prototype was realized for testing the proposed acquisition strategy. Several tests involving the acquisition of different waveforms, including the vibration signal's reproductions and FFT computations, were carried out on the DAQ prototype, thus validating the system's capability of capturing vibration signals. The DAQ's sampling frequency is 12.5 kHz for dual-channel operation and 22.2 kHz when utilizing only one acquisition channel. Moreover, the board computes the FFT of vibrational data, storing them on the micro-SD card.

A comparative analysis of the proposed DAQ board with solutions reported in the literature was performed, demonstrating higher flexibility and wider functionalities than similar reported in the scientific literature and comparable with those of the commercial DAQs for vibration analysis, although at a reduced cost (EUR 400–500).

Moreover, future firmware versions could include an onboard digital filter implementation and wireless data transmission. Additional future developments could include support for multi-core microcontrollers to perform tasks in parallel or the employment of FPGAs, both viable strategies to improve the sampling frequency. In particular, a custom board based on the footprint of the Blackpill could be designed, employing multi-core MCUs or FPGAs.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/electronics13071187/s1, File S1: Bill of Materials for assembling the developed DAQ board; File S2: DAQ board code.

Author Contributions: Conceptualization, R.D.F., L.S., A.M. and P.V.; investigation, R.D.F., L.S., A.M. and P.V.; resources, P.V. and A.M.; data curation, R.D.F., L.S. and P.V.; writing—original draft preparation, R.D.F., L.S., A.M. and P.V.; writing—review and editing, R.D.F. and P.V.; visualization, R.D.F. and P.V.; supervision, R.D.F., A.M. and P.V.; funding acquisition, P.V. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data of our study are available upon request.

Conflicts of Interest: The authors declare no conflicts of interest.

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